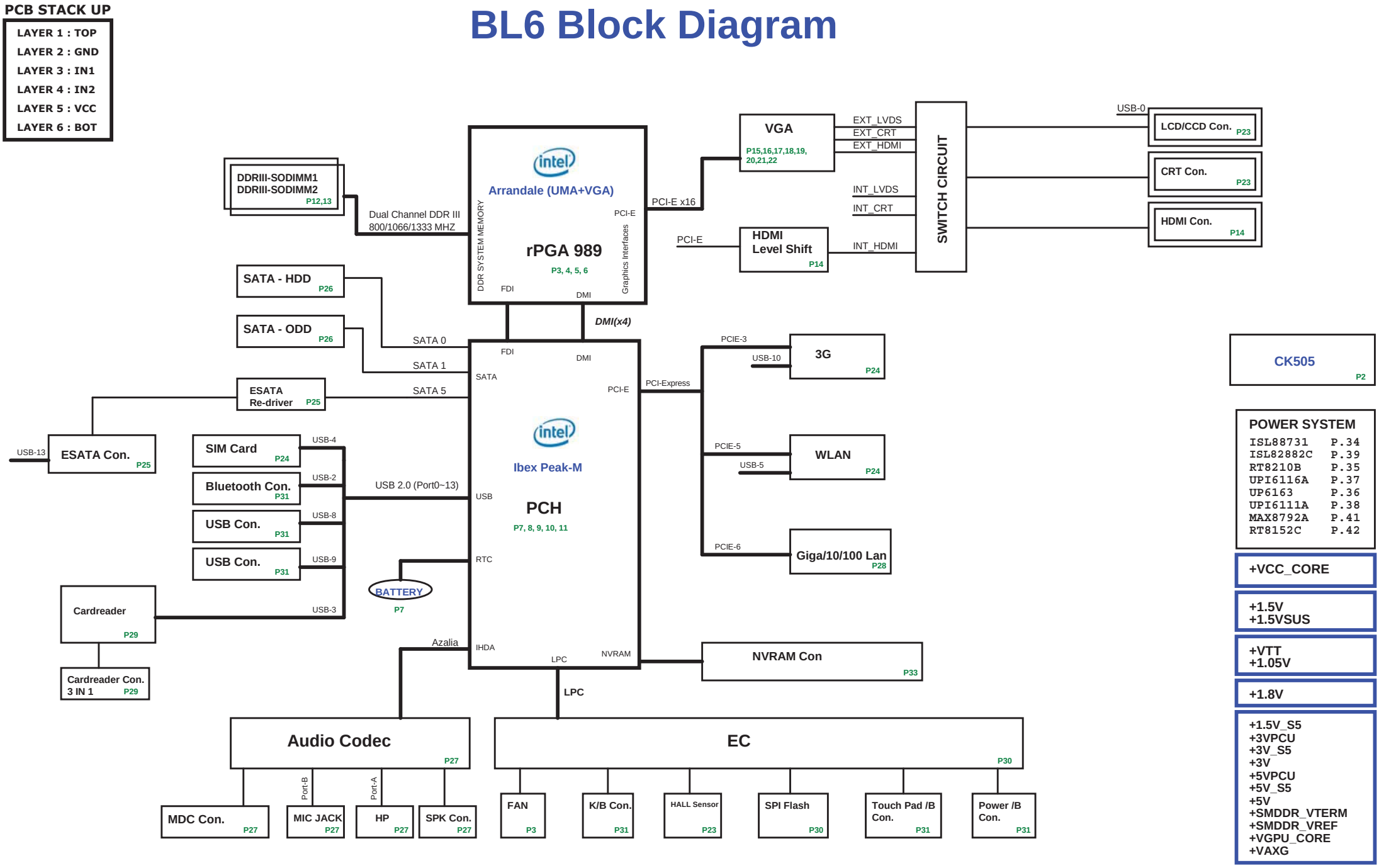
BL6 Block Diagram



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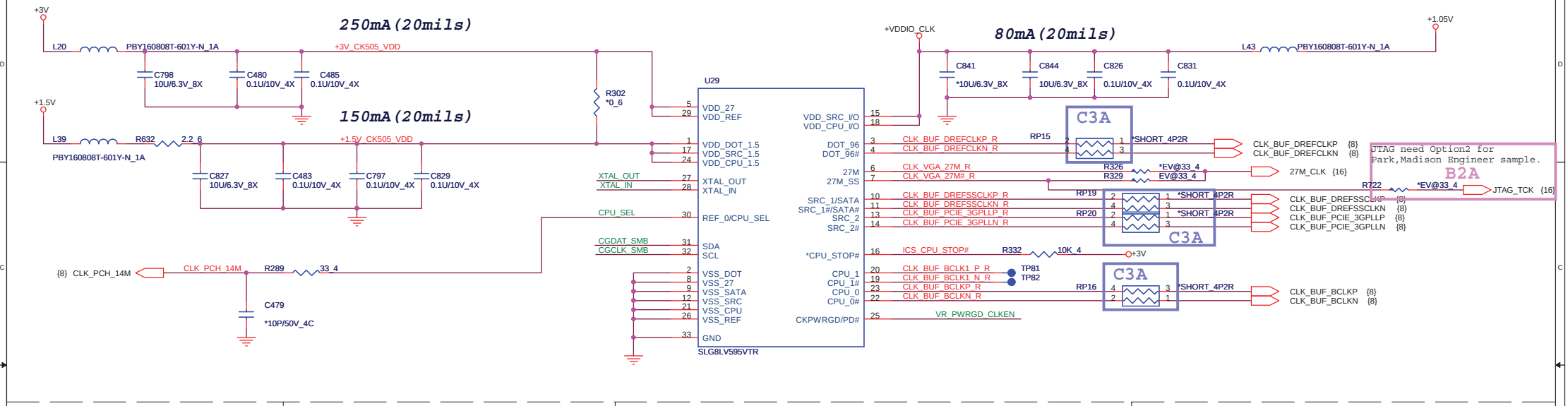
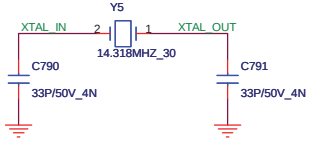
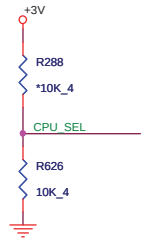
CLOCK Gen



CLK CRYSTAL

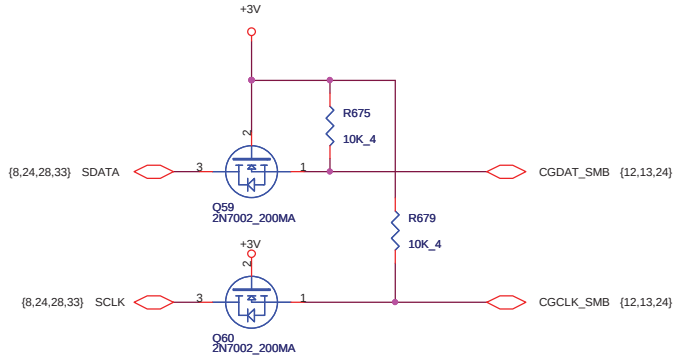


CLK CPU_SEL



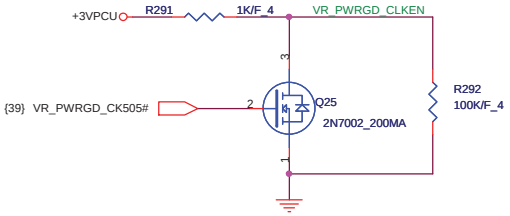
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

Change to +3VPCU
(follow CRB)



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PROJECT : BL6

Size	Document Number	Rev
	CLOCK GENERATOR	A1A

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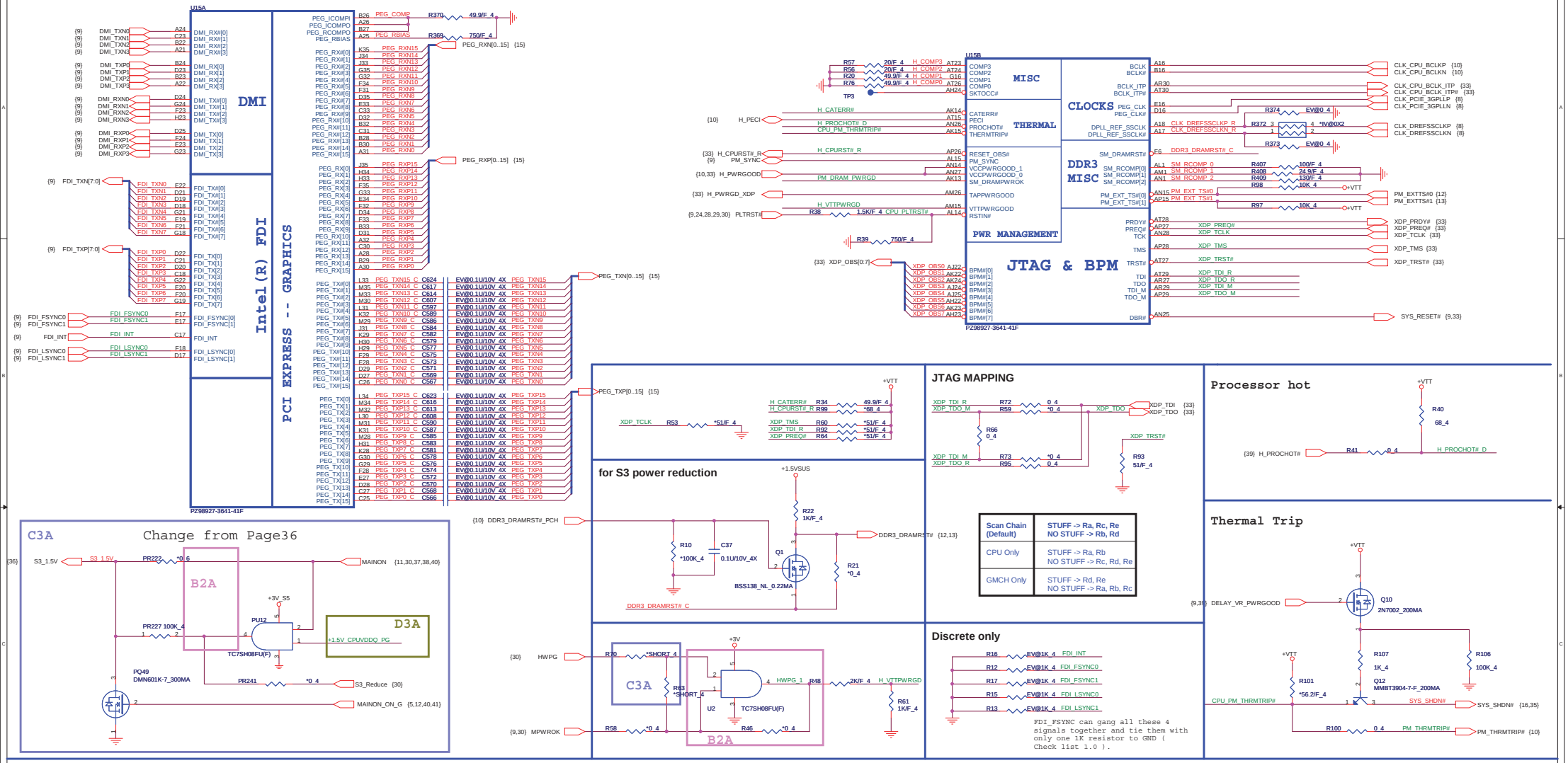

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable

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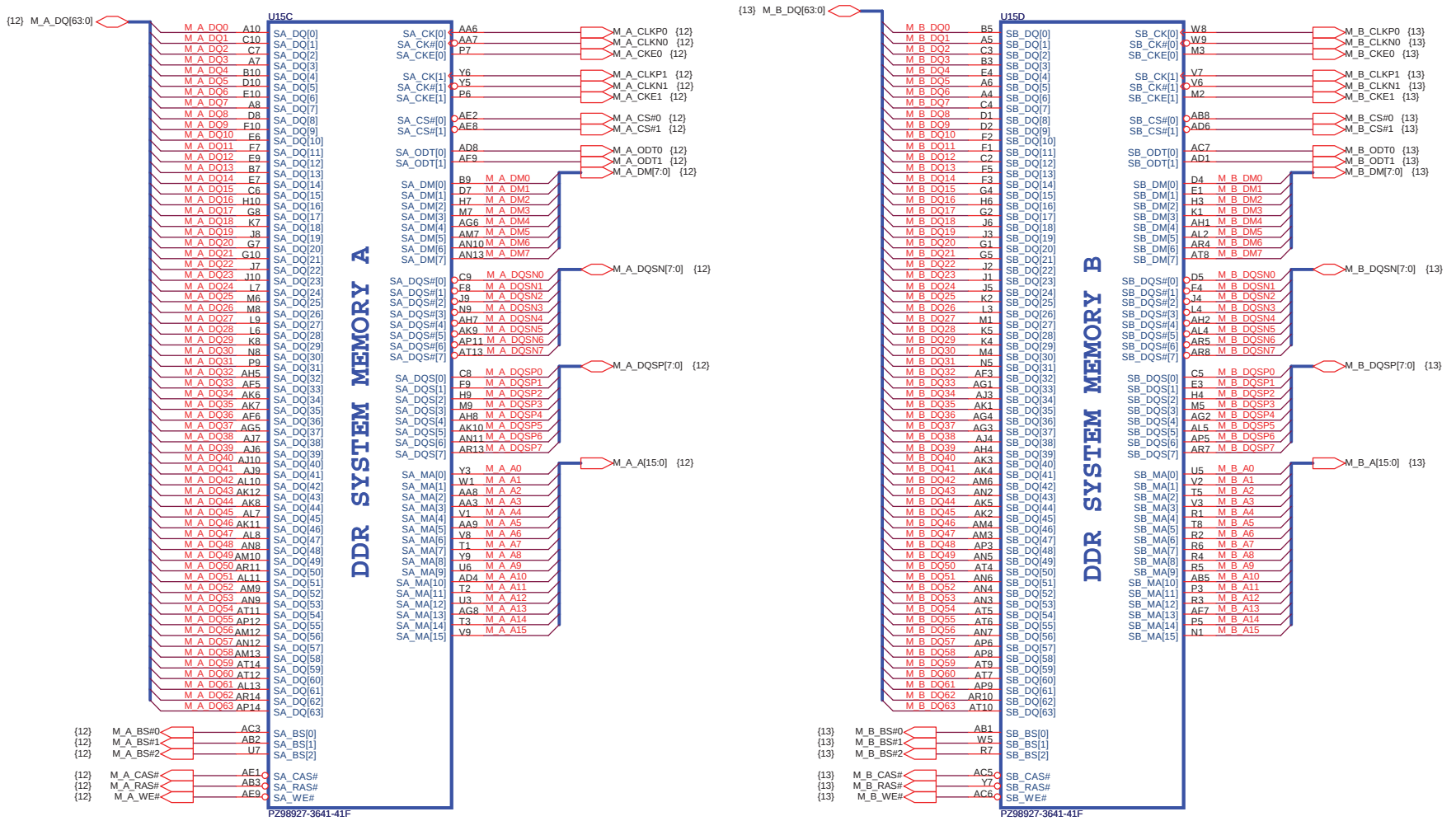
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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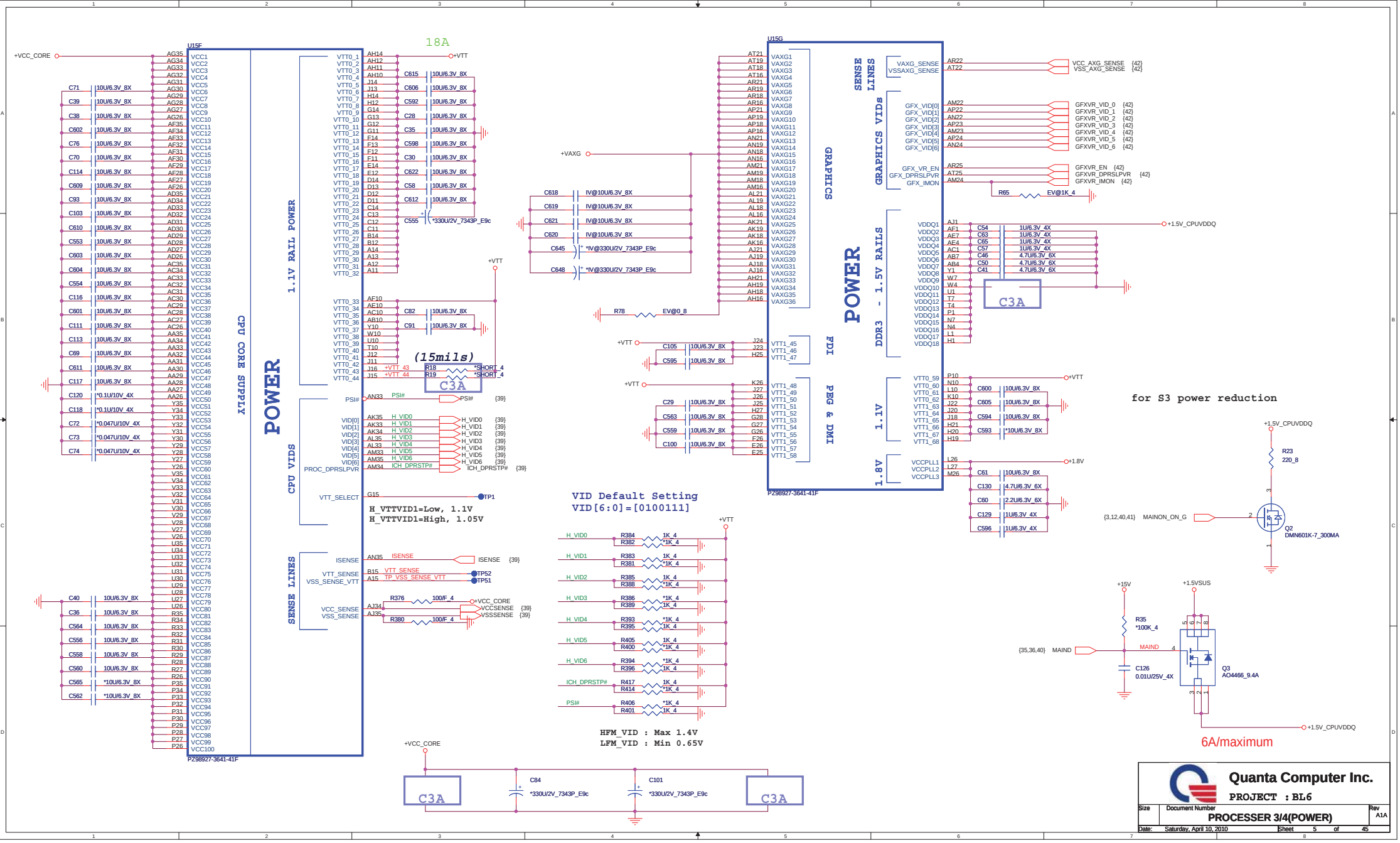
PROJECT : BL6

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	A1A

Date: Saturday, April 10, 2010 Sheet 4 of 45



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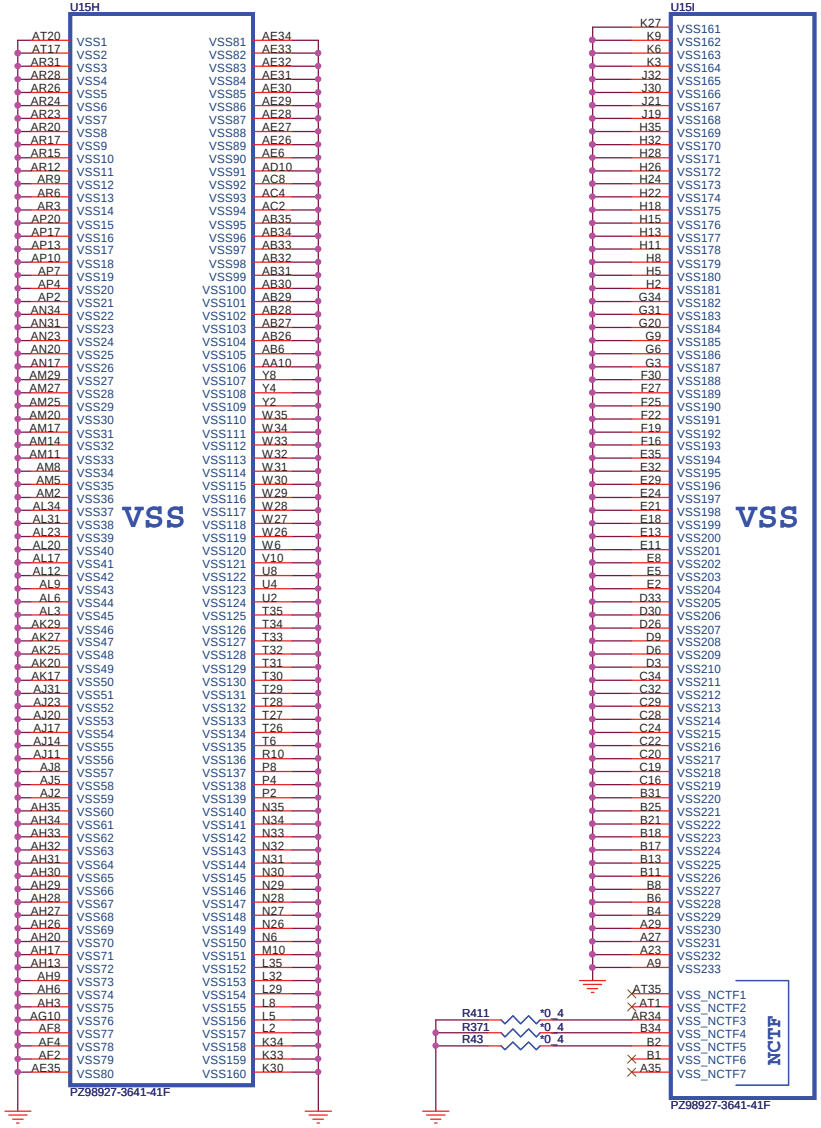
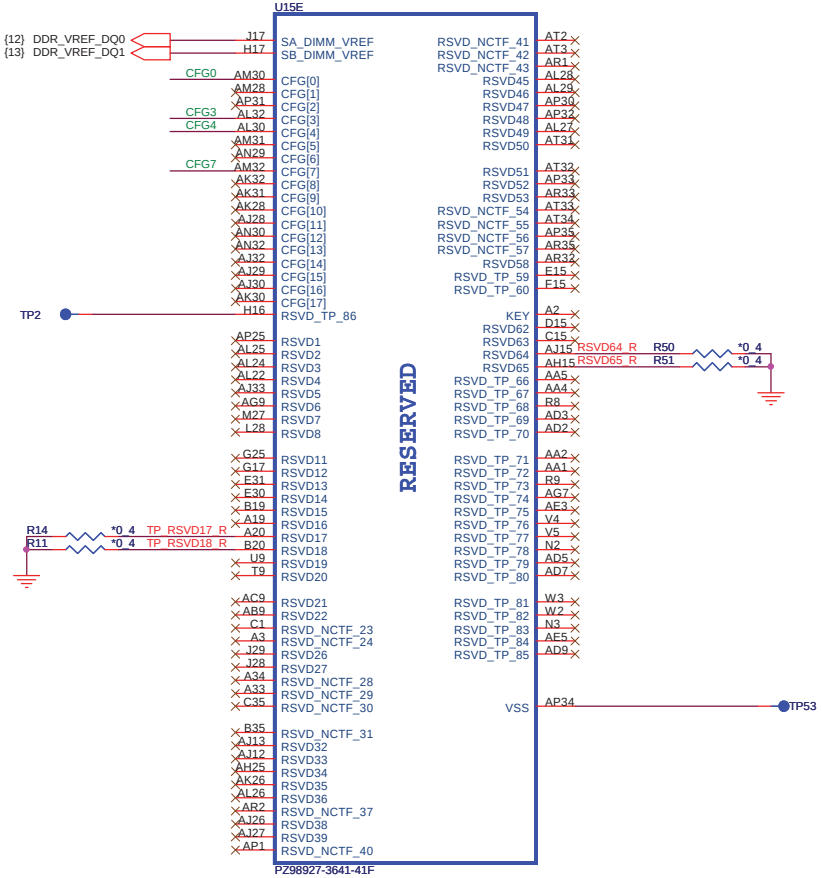
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Express Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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PROJECT : BL6

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

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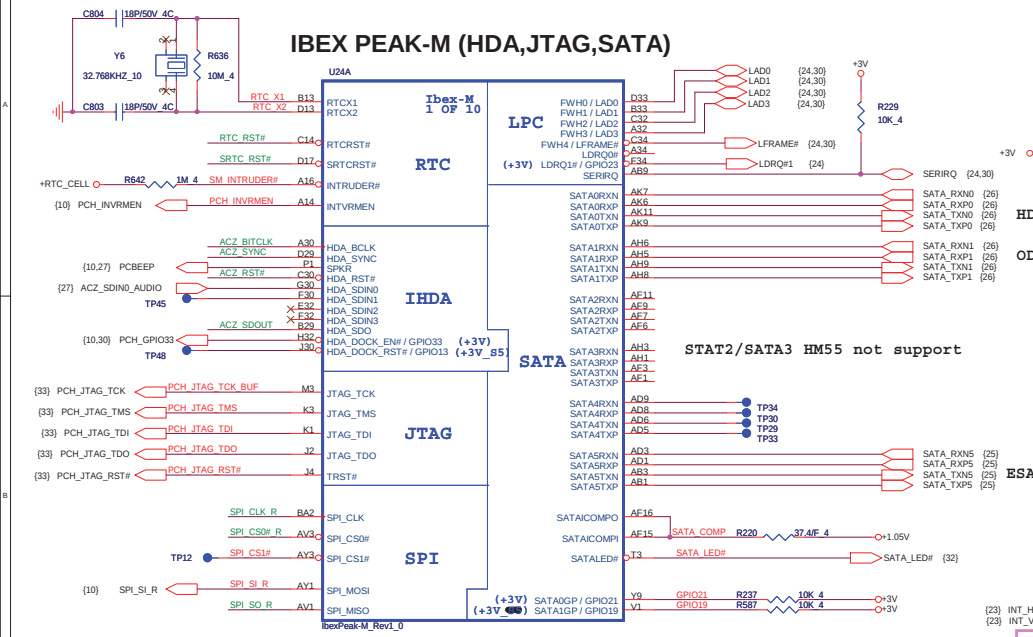
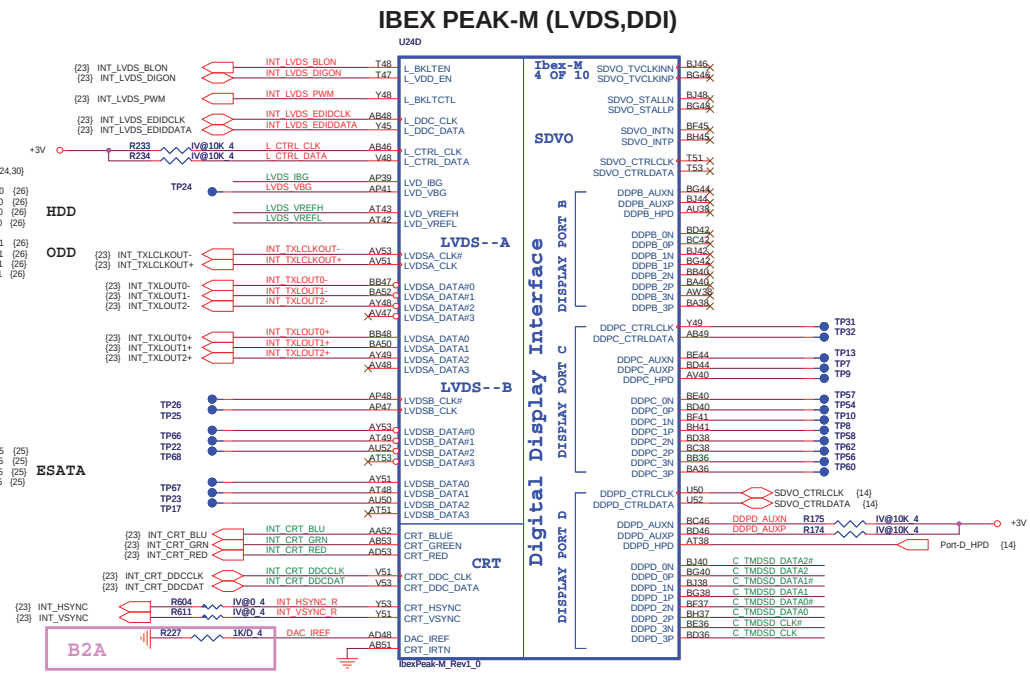
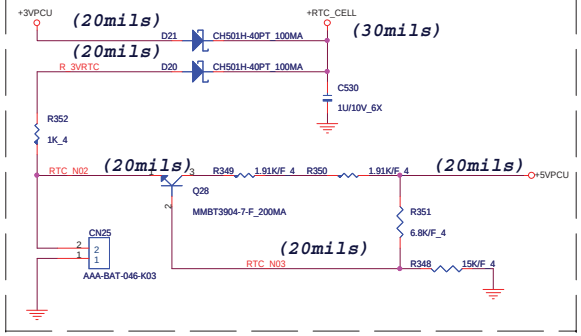
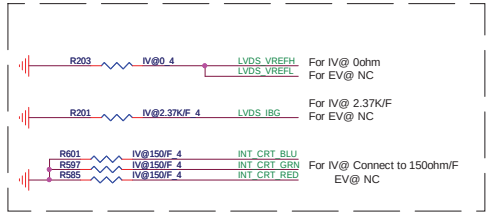


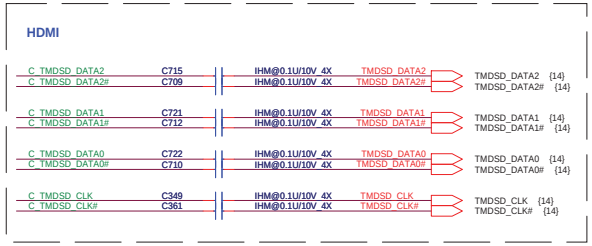


Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

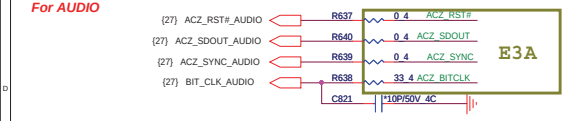
RTC BATTERY

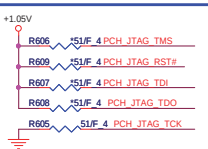






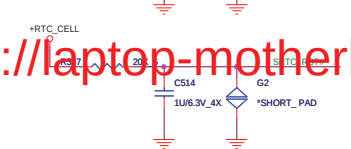
For AUDIO





RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM

PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

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PROJECT : BL6

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	A1A

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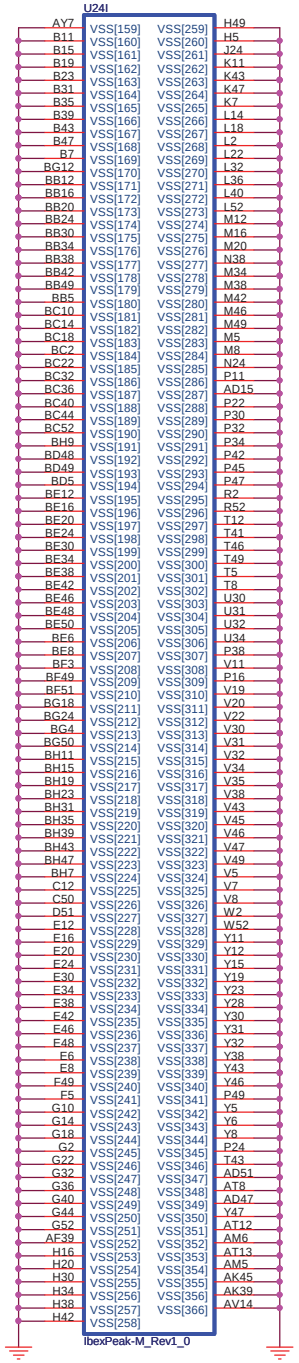
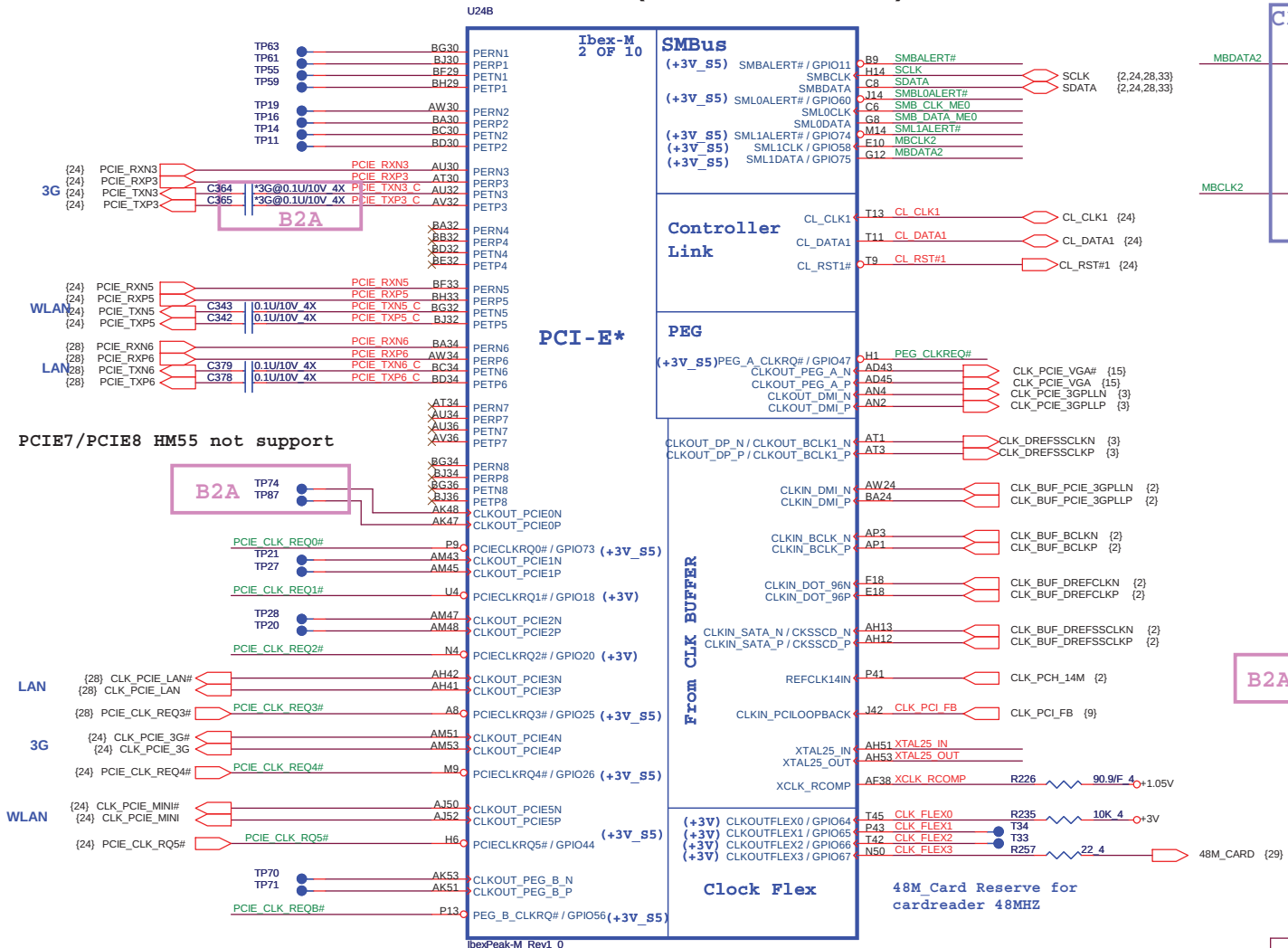
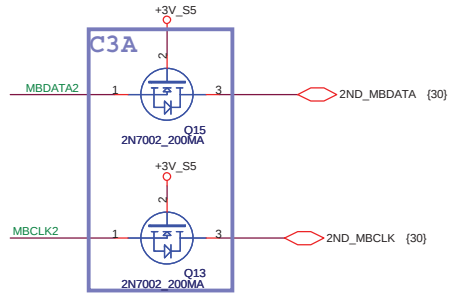
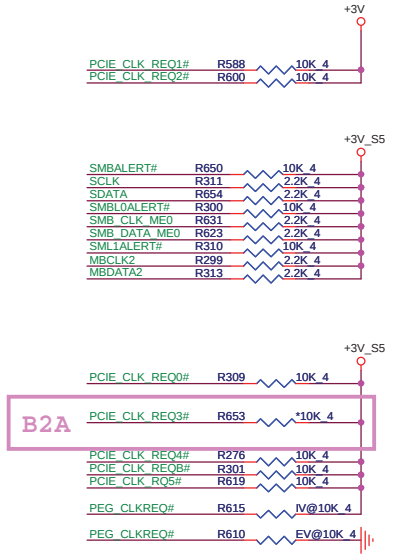
IBEX PEAK-M (GND)



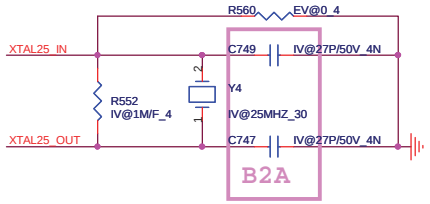
IBEX PEAK-M (PCI-E,SMBUS,CLK)







Placement close



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Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	PCH 2/5 (PCIE, SMBUS, CK)	A1A
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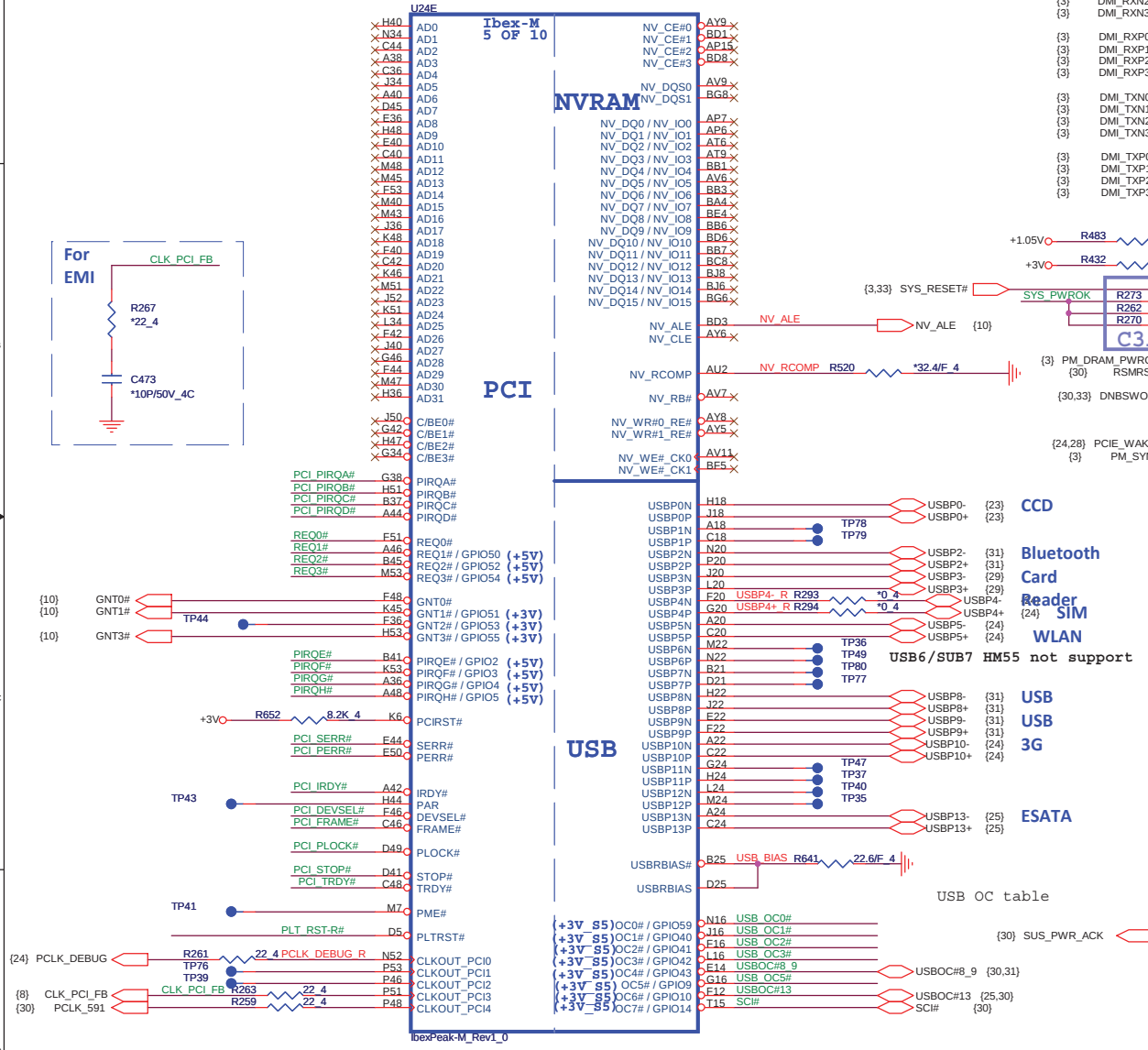
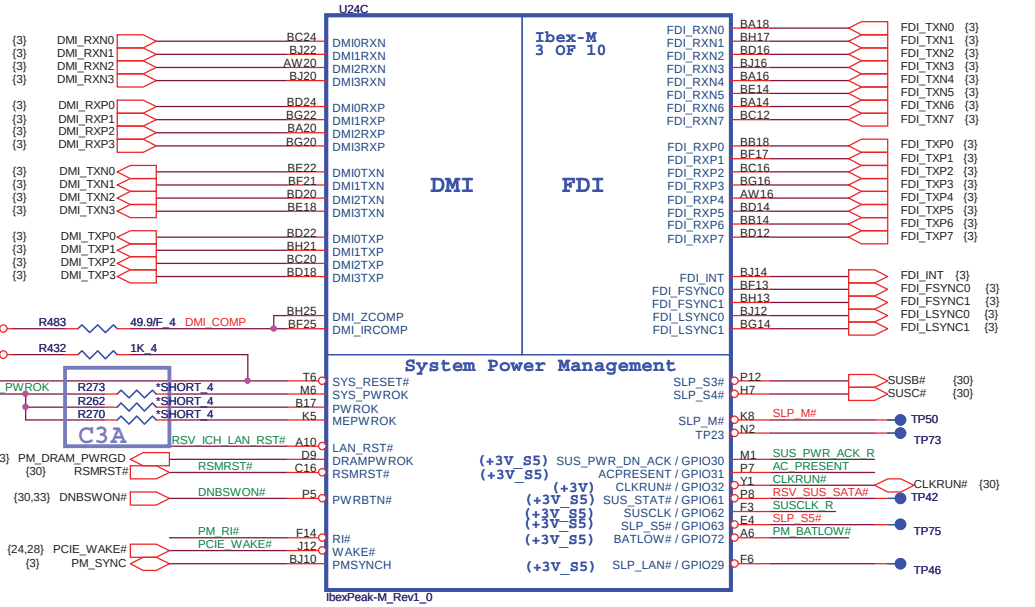
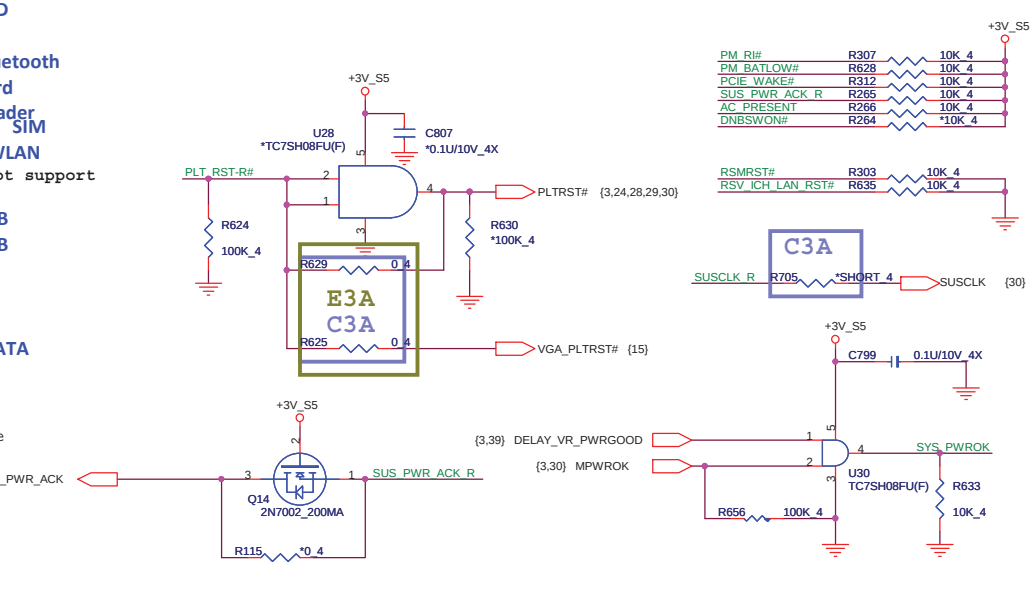
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)





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PROJECT : BL6

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	A1A

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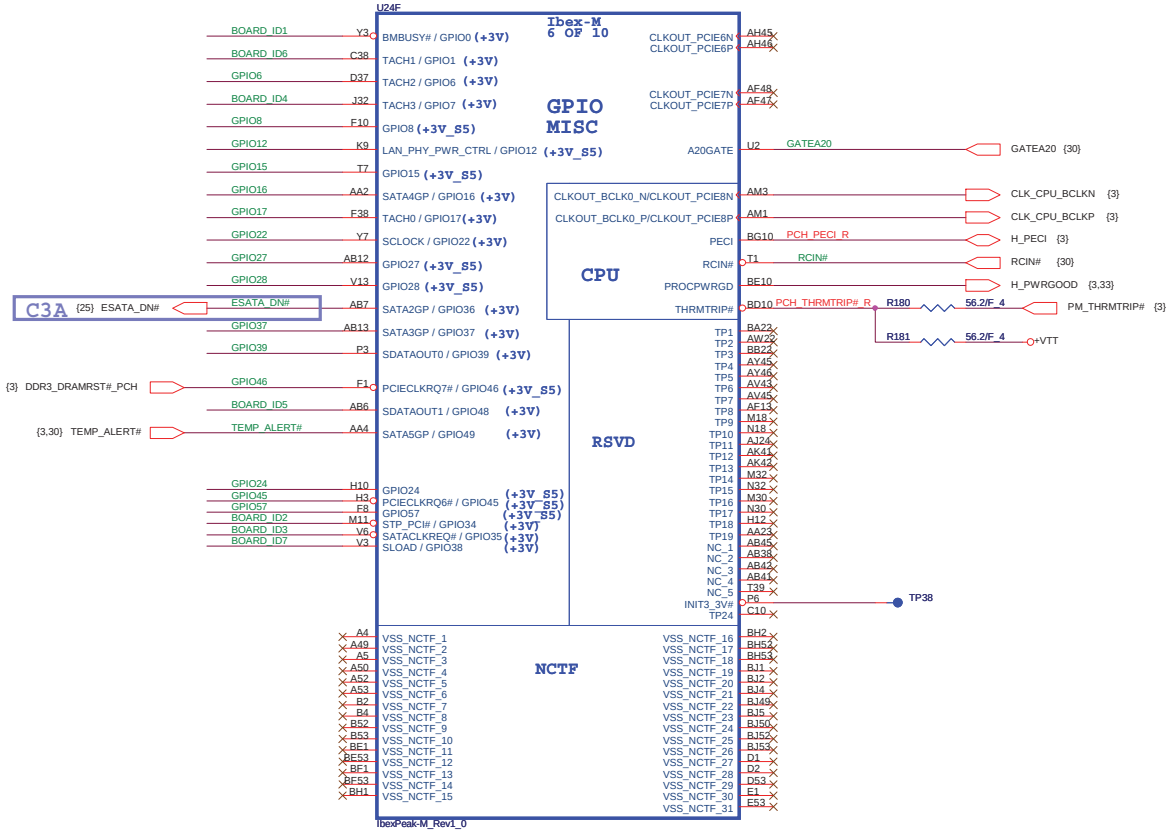
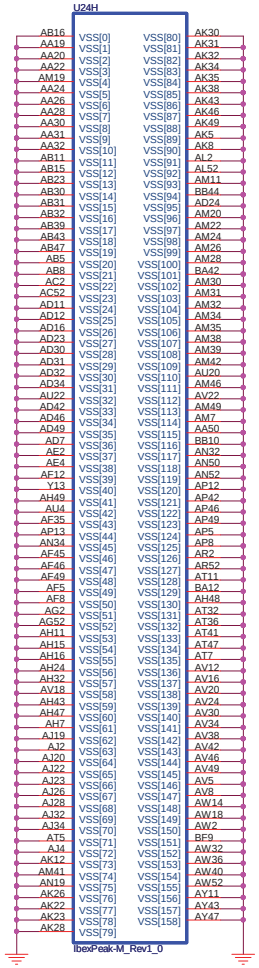
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

{7,27} PCBEEP — R592 *1K_4 — +3V

Reboot option at power-up

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

{9} GNT3# — R622 *10K_4

Top-Block Swap Override

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

HDA_DOCK_EN #/GPIO33

{7,30} PCH_GPIO33 — R282 1K_4 — E3A — JP1 2 — *SHORT PAD 1

Flash Descriptor Security Override

0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

GNT0#, GNT1#

{9} GNT0# — GNT0# R272 *1K_4
{9} GNT1# — GNT1# R621 *1K_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

SPI_MOSI

{7} SPI_SI_R — R504 *1K_4 — +3V

TPM Functionality Disable

1 = Enabled
0 = Disable

NV_ALE

{9} NV_ALE — R496 *10K_4 — +1.8V

IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R298 10K_4 — +3V_S5

Reserved

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R248 1K_4 — +3V_S5

Reserved

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

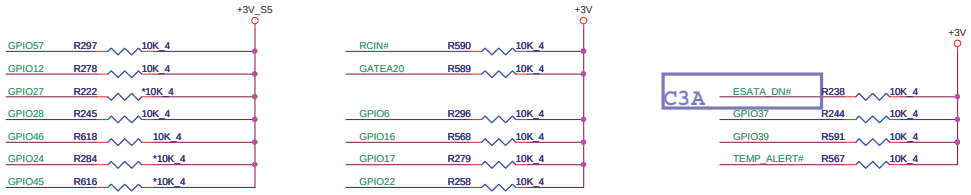
GPIO27 — R232 *10K_4

On-Die PLL Voltage Regulator

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

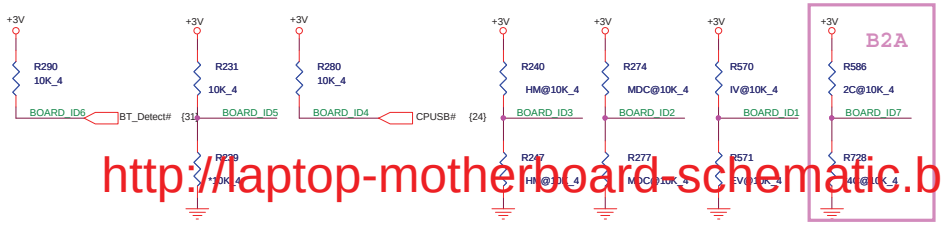
+RTC_CELL — R644 330K_6 — PCH_INVRMEN — PCH_INVRMEN {7}

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU VGA SKU	H L						
W/ MDC W/O MDC		H L					
W/ HDMI W/O HDMI			H L				
W/O 3G W/ 3G				H L			
15" 14"					H L		
W/O BT W/ BT						H L	
2 Core 4 Core							H L



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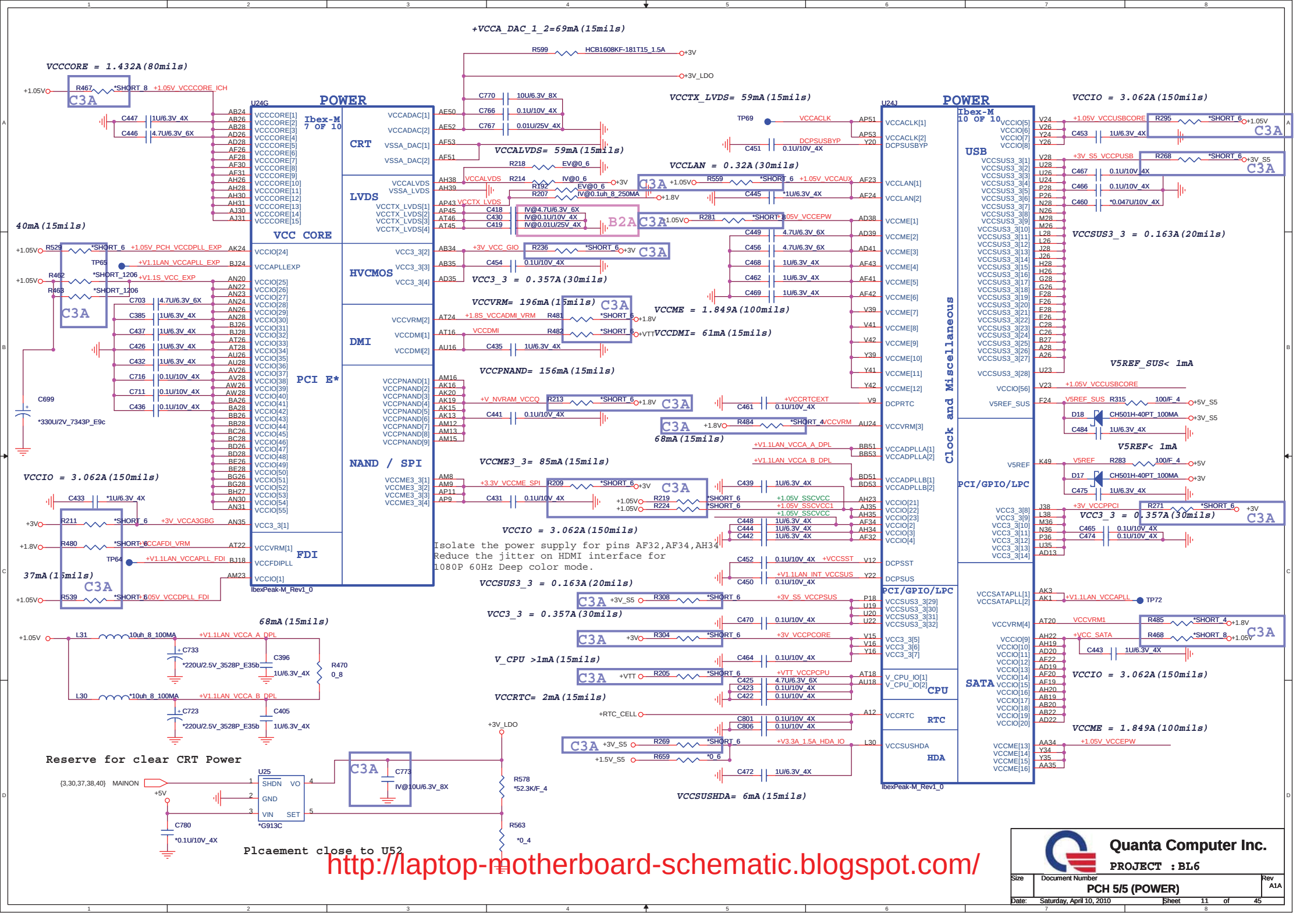
Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	A1A

Date: Saturday, April 10, 2010 Sheet 10 of 45


POWER
Ibex-M 7 OF 10
U24G
VCC CORE
PCI E*
FDI
CRT
LVDS
HVCMOS
DMI
NAND / SPI
IbexPeak-M_Rev1_0
POWER
Ibex-M 10 OF 10
U24J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IbexPeak-M_Rev1_0
+VCCA_DAC_1_2=69mA(15mils)
VCCCORE = 1.432A(80mils)
VCCTX_LVDS= 59mA(15mils)
VCCALVDS= 59mA(15mils)
VCCLAN = 0.32A(30mils)
VCCIO = 3.062A(150mils)
VCCSUS3_3 = 0.163A(20mils)
40mA(15mils)
VCC3_3 = 0.357A(30mils)
VCCVRM= 196mA(15mils)
VCCME = 1.849A(100mils)
VCCDMI= 61mA(15mils)
VCCPNAND= 156mA(15mils)
68mA(15mils)
VCCME3_3= 85mA(15mils)
VCCIO = 3.062A(150mils)
Isolate the power supply for pins AF32,AF34,AH34
Reduce the jitter on HDMI interface for
1080P 60Hz Deep color mode.
VCCSUS3_3 = 0.163A(20mils)
VCC3_3 = 0.357A(30mils)
V_CPU >1mA(15mils)
VCCRTC= 2mA(15mils)
VCCSUSHDA= 6mA(15mils)
V5REF_SUS< 1mA
V5REF< 1mA
VCC3_3 = 0.357A(30mils)
VCCIO = 3.062A(150mils)
VCCME = 1.849A(100mils)
37mA(15mils)
68mA(15mils)
Reserve for clear CRT Power
Plcaement close to U52
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Quanta Computer Inc.
PROJECT : BL6
Size
Document Number
PCH 5/5 (POWER)
Rev
A1A
Date: Saturday, April 10, 2010
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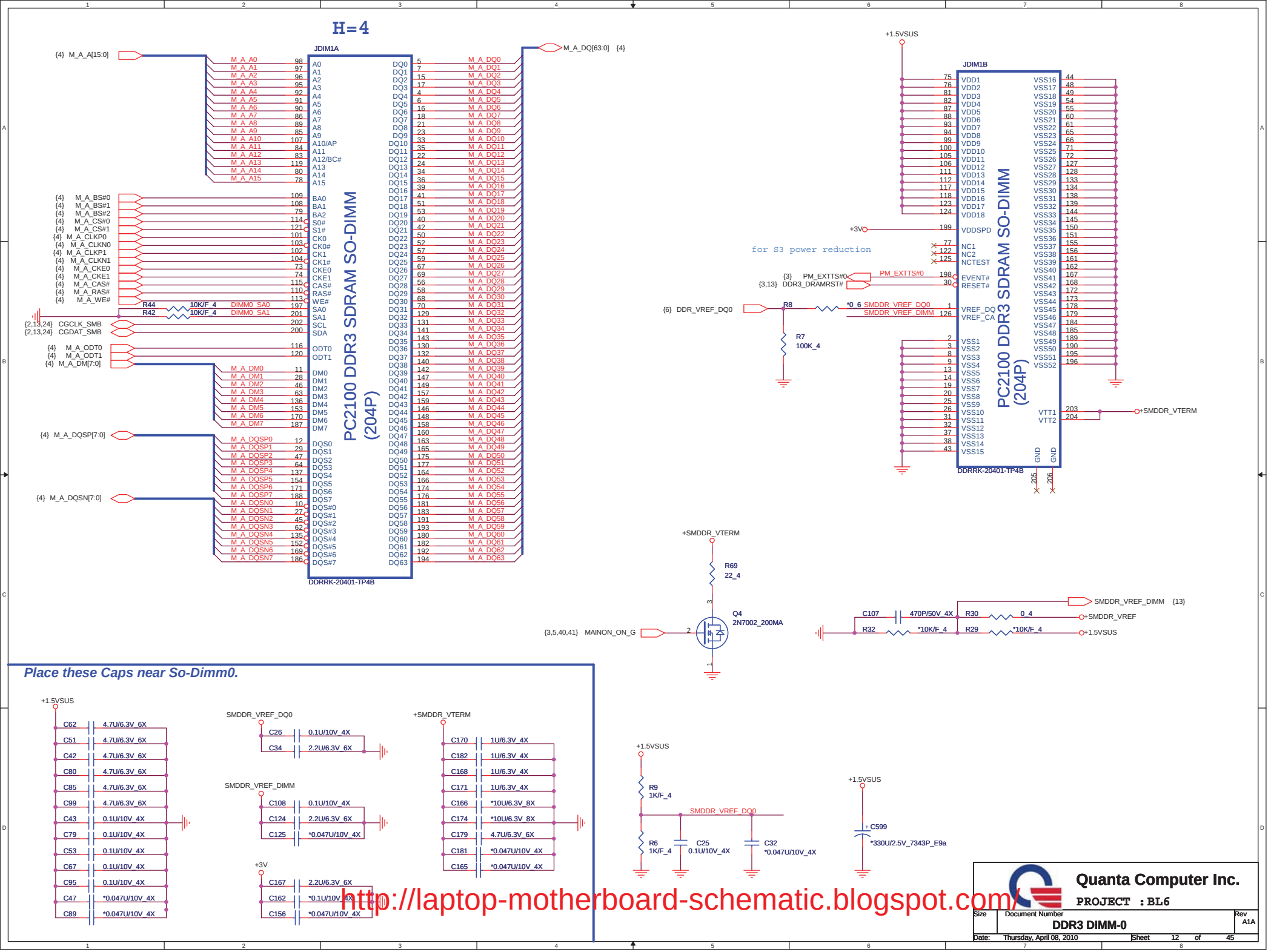

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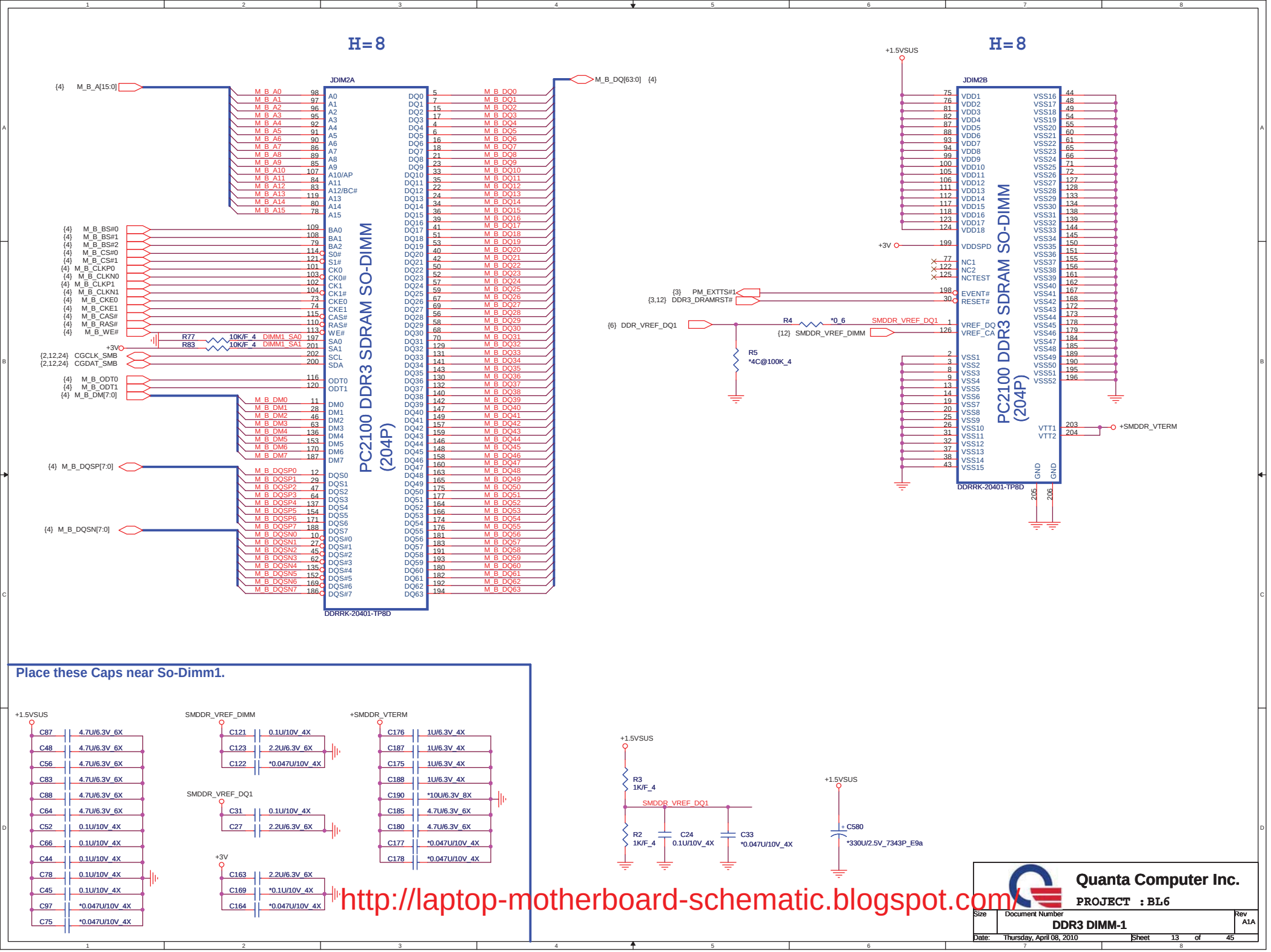
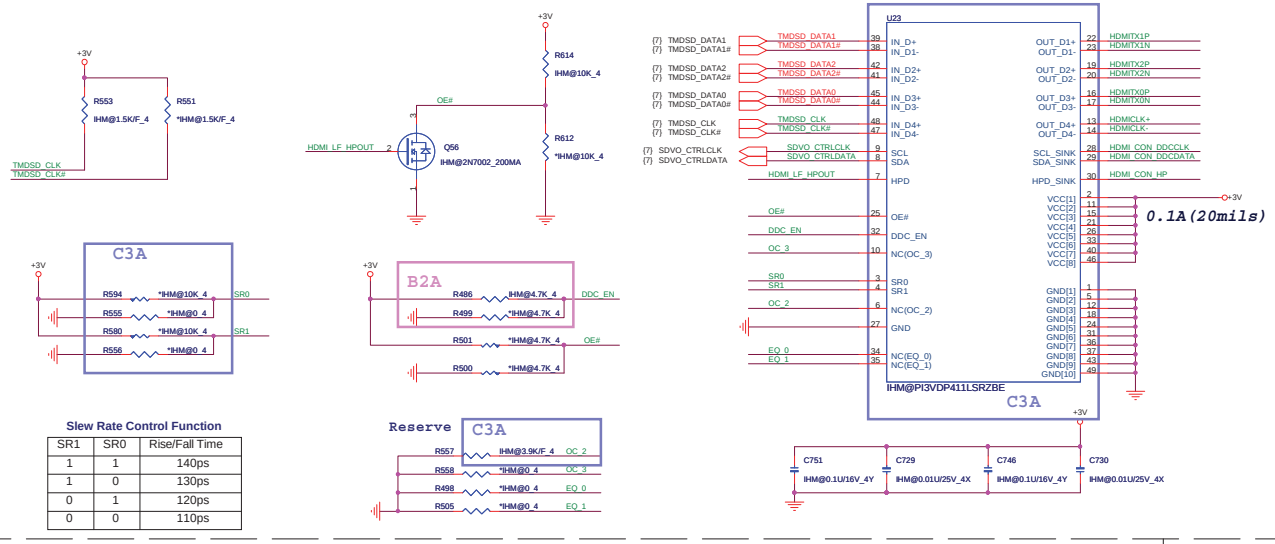


http://laptop-motherboard-schematic.blogspot.com/

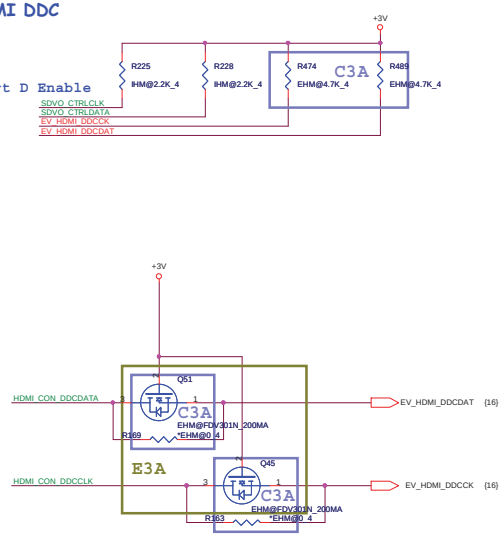
HDMI Level Shift



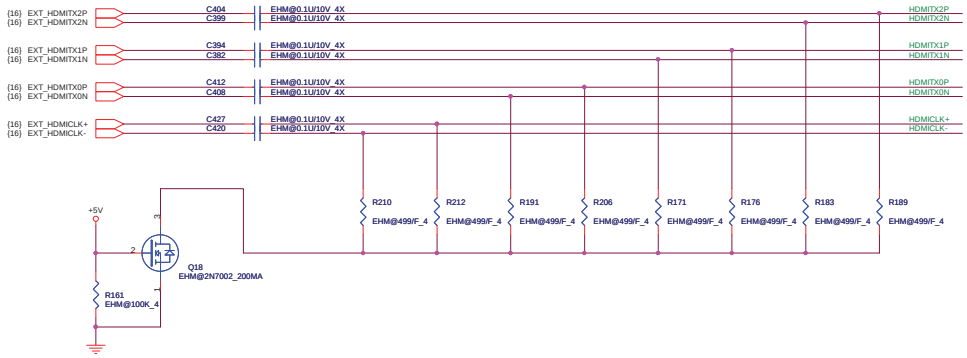
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

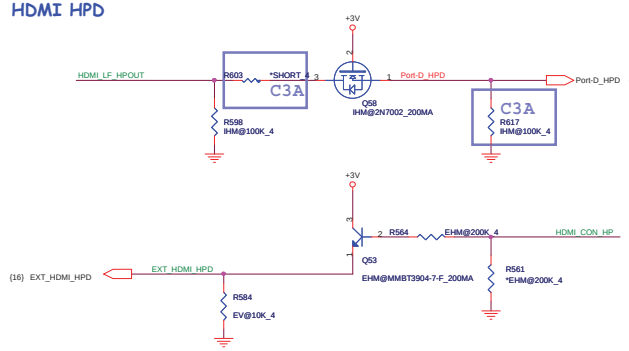
HDMI DDC

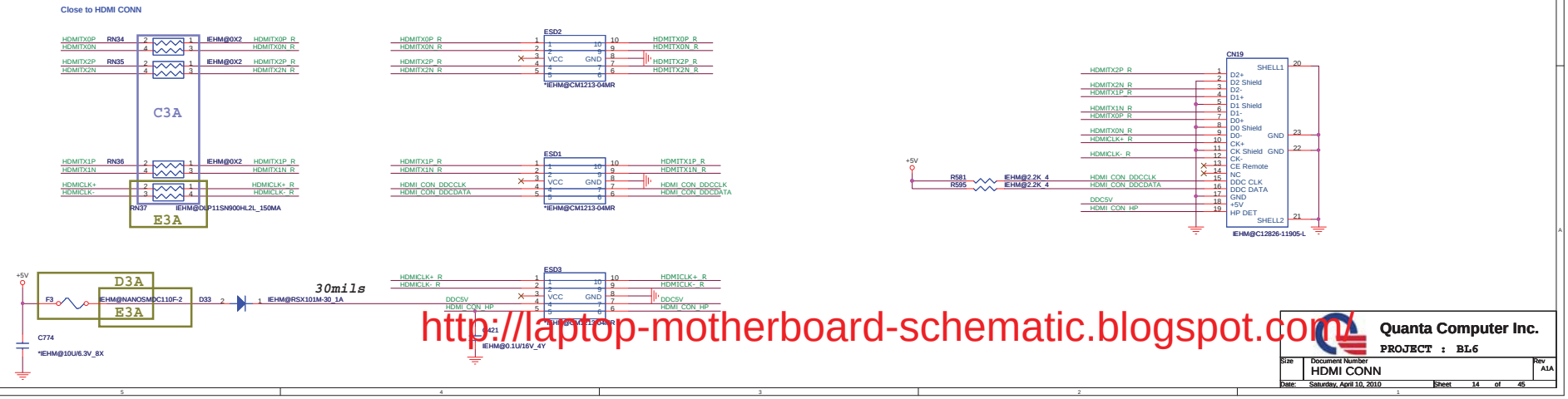


Discrete HDMI



HDMI HPD





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Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	HDMI CONN	A1A

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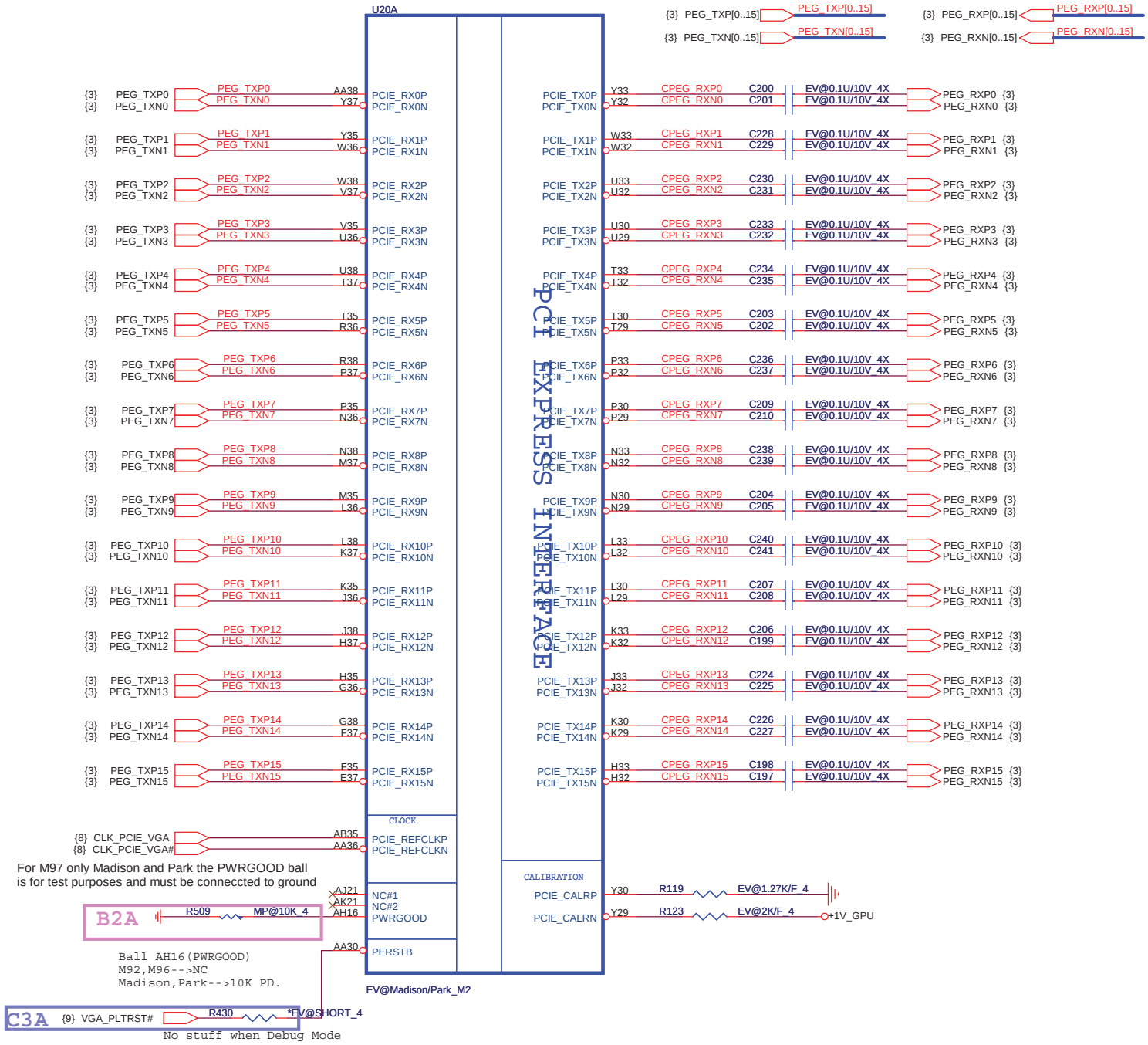

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PROJECT : BL6

Size	Document Number	Rev
	Madison/Park-HOST I/F	A1A

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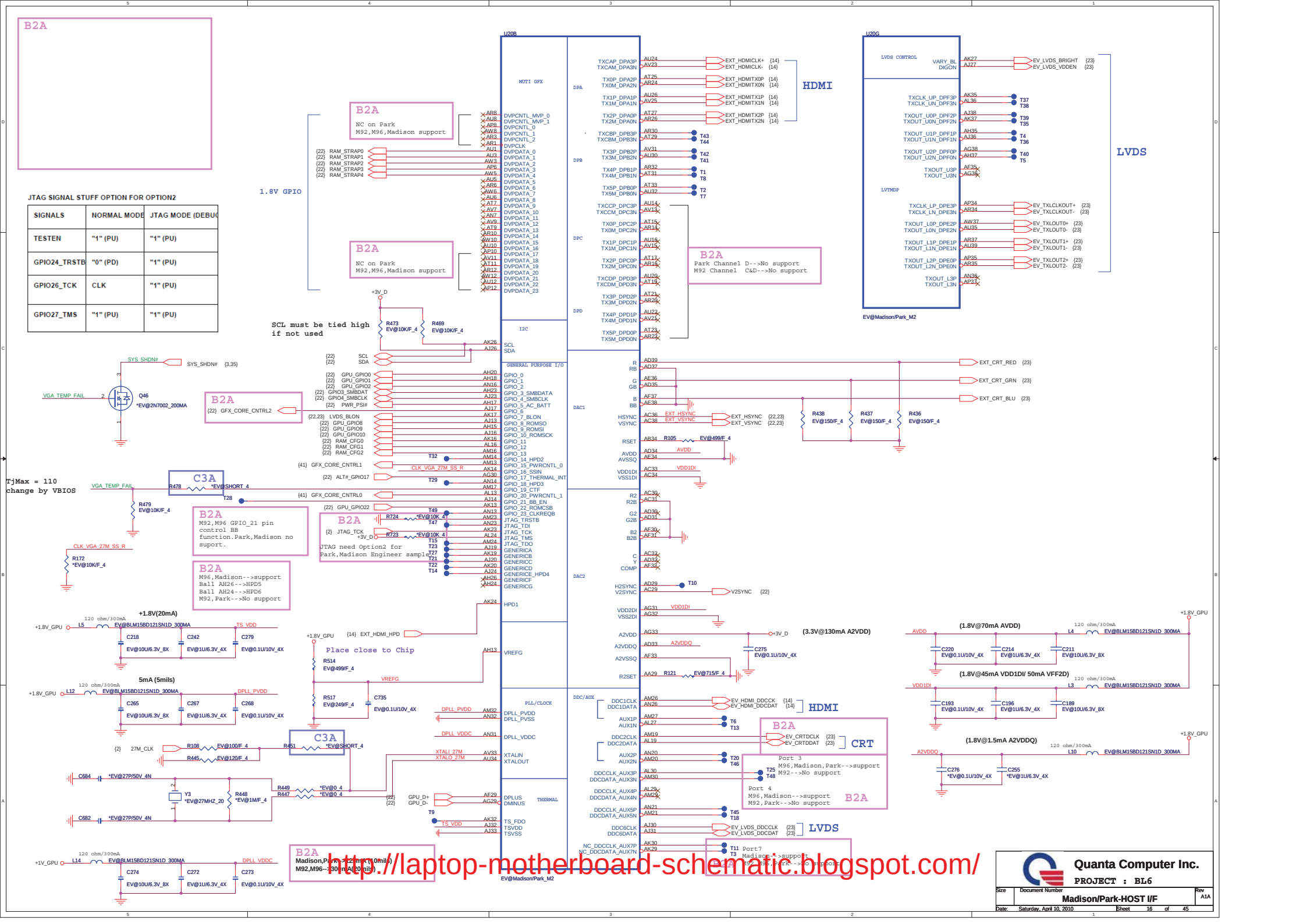
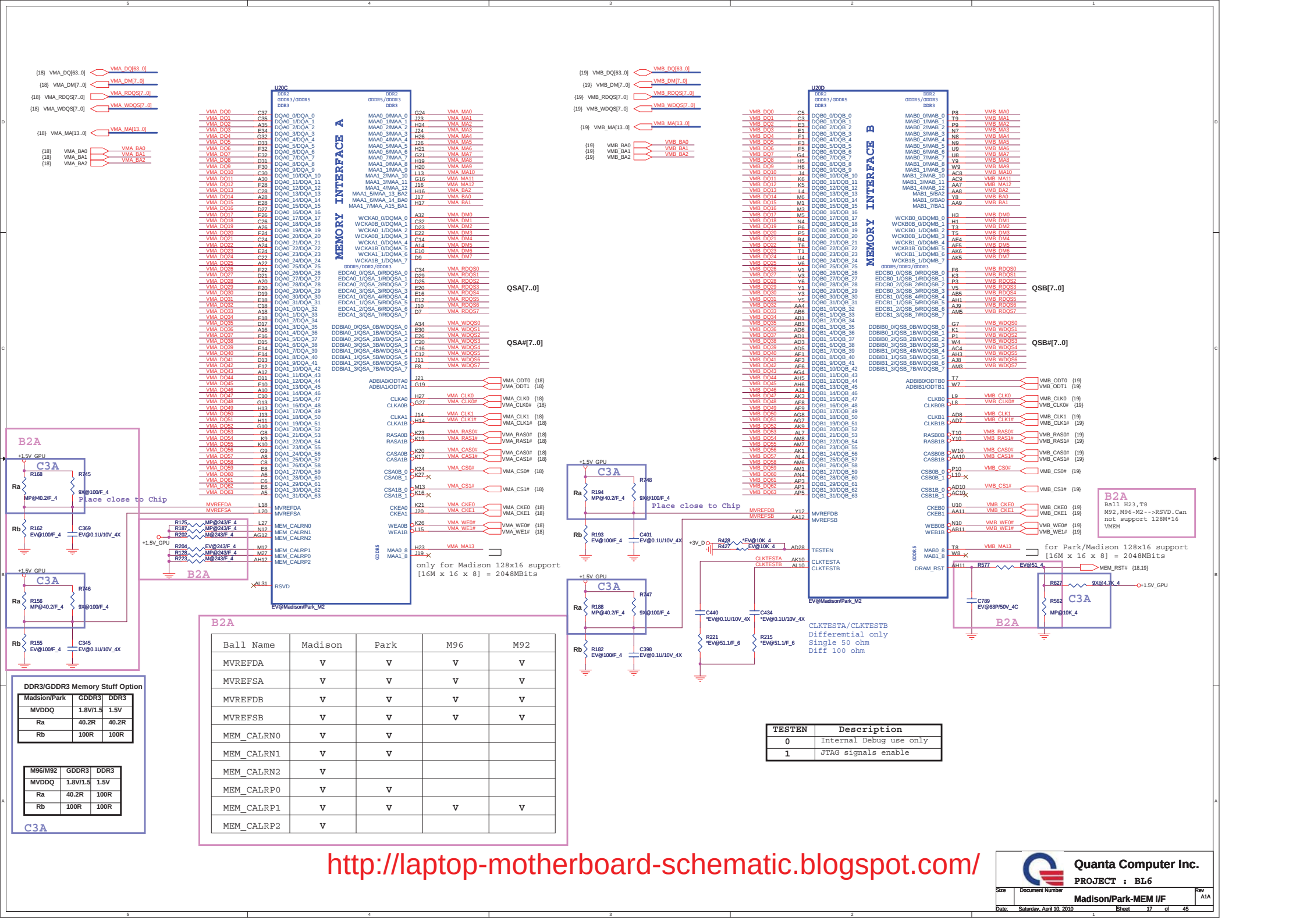


http://laptop-motherboard-schematic.blogspot.com/



Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

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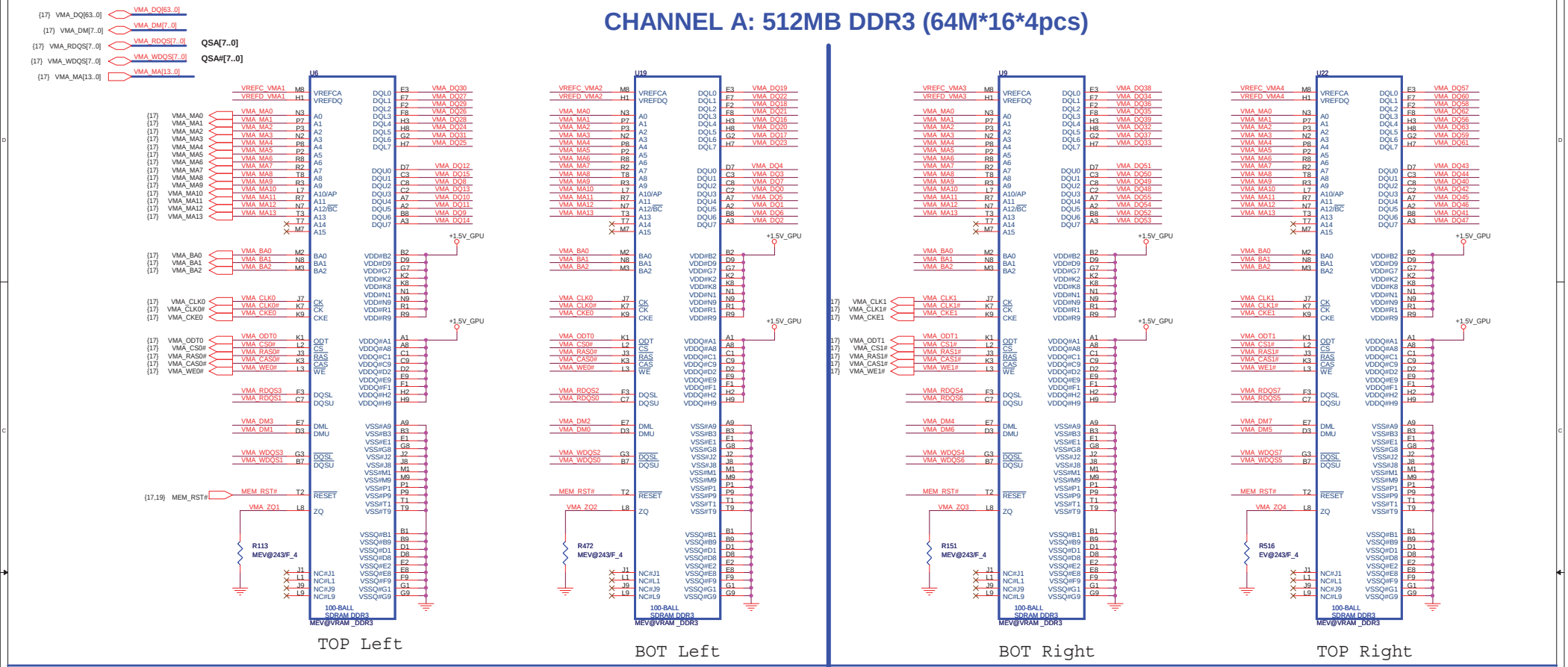
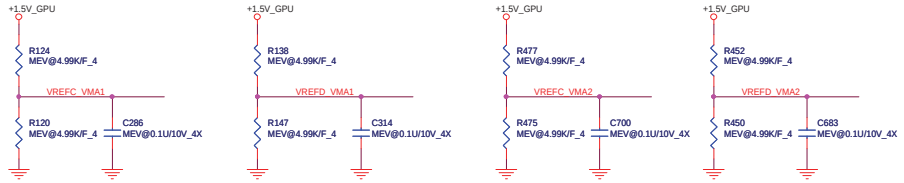
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



Group-A0 VREF



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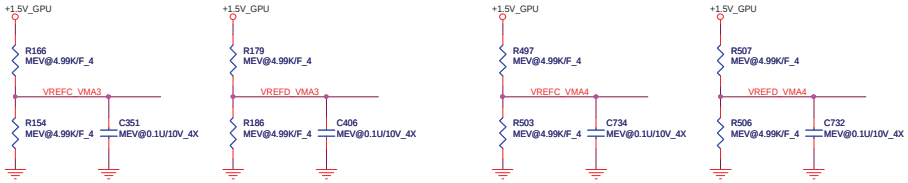
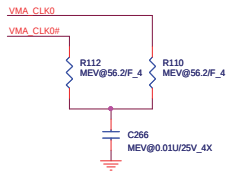


MEM_A0 CLK



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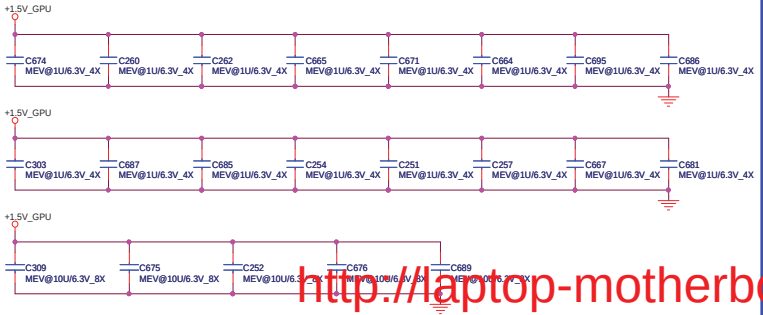
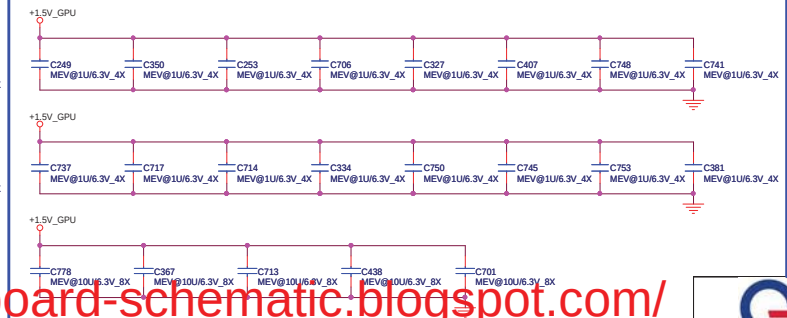
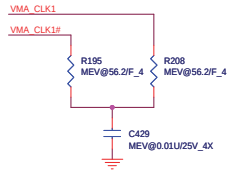


Group-A1 decoupling CAP



MEM_A1 CLK



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Size	Document Number	Rev
	VRAM_A: DDR3-64M*16*4PCS	A1A

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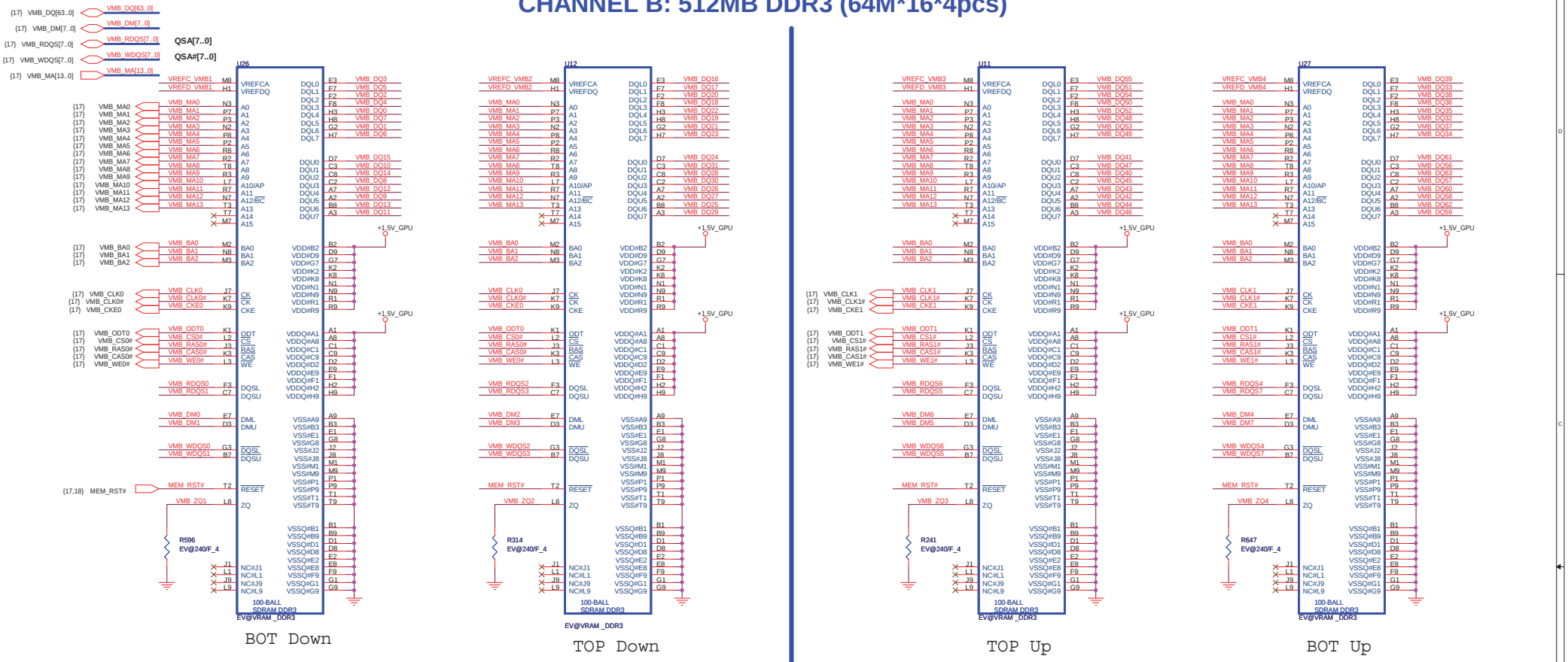
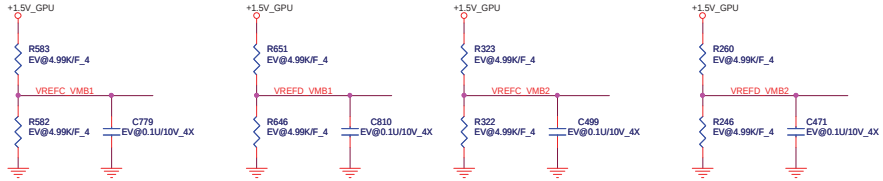
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



Group-B0 VREF



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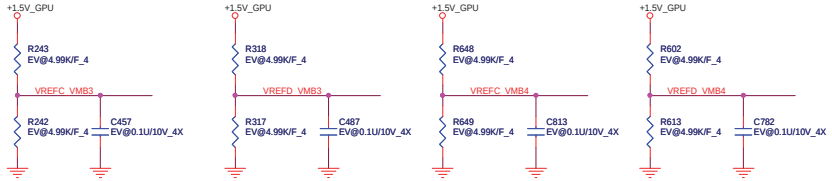
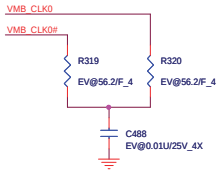
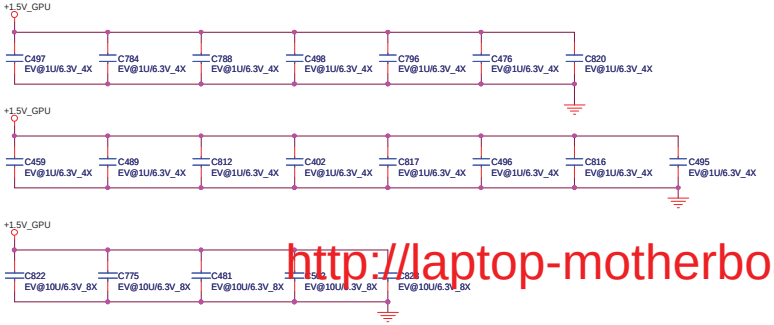


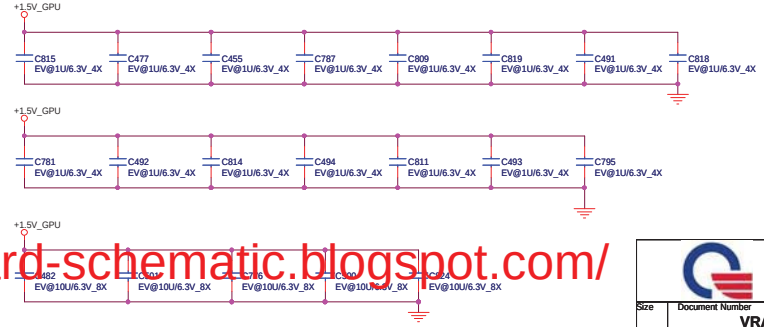
MEM_B0 CLK



Group-B0 decoupling CAP



Group-B1 decoupling CAP



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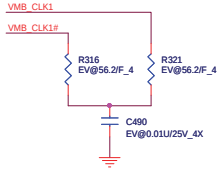

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Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	A1A

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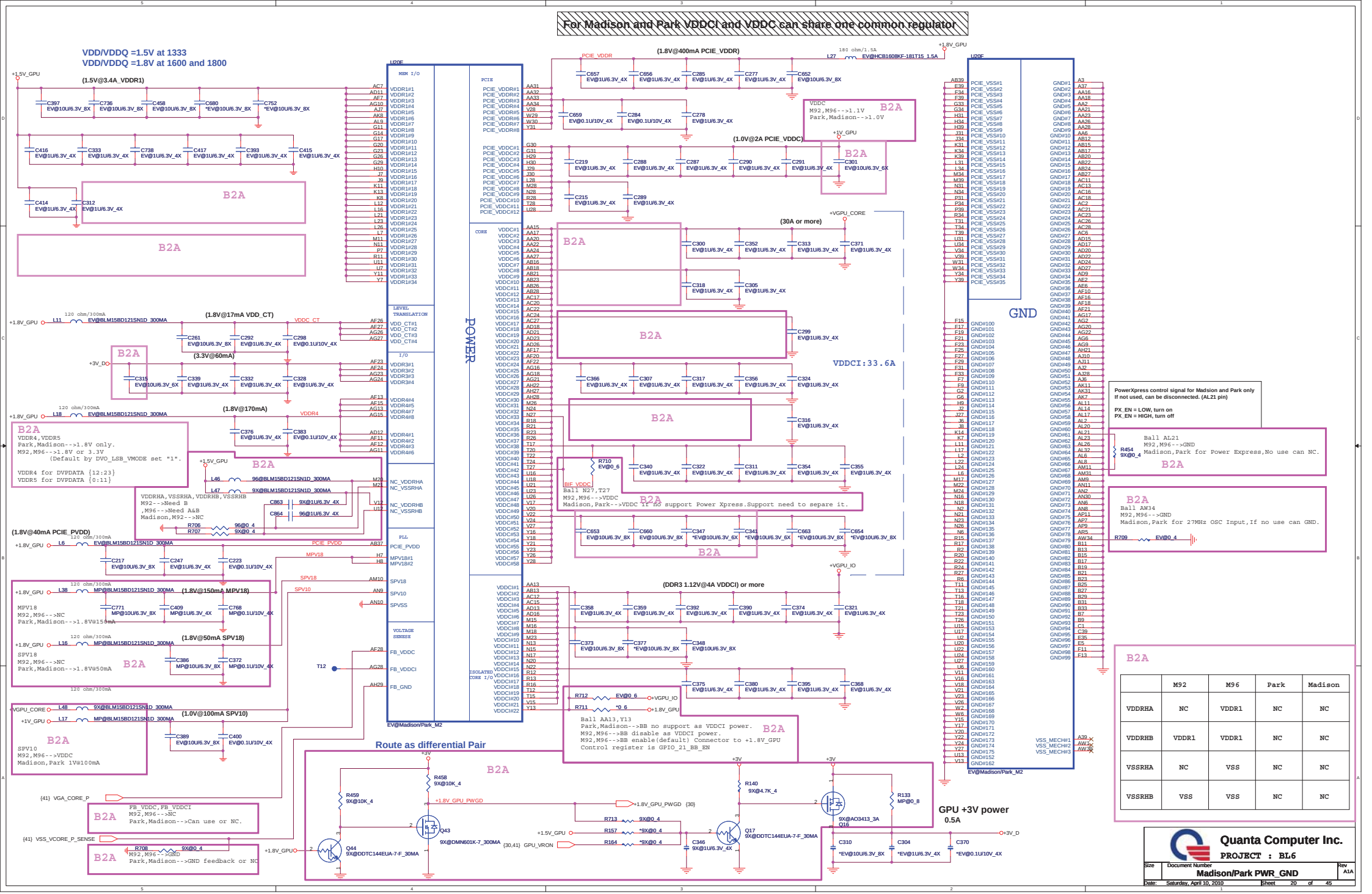
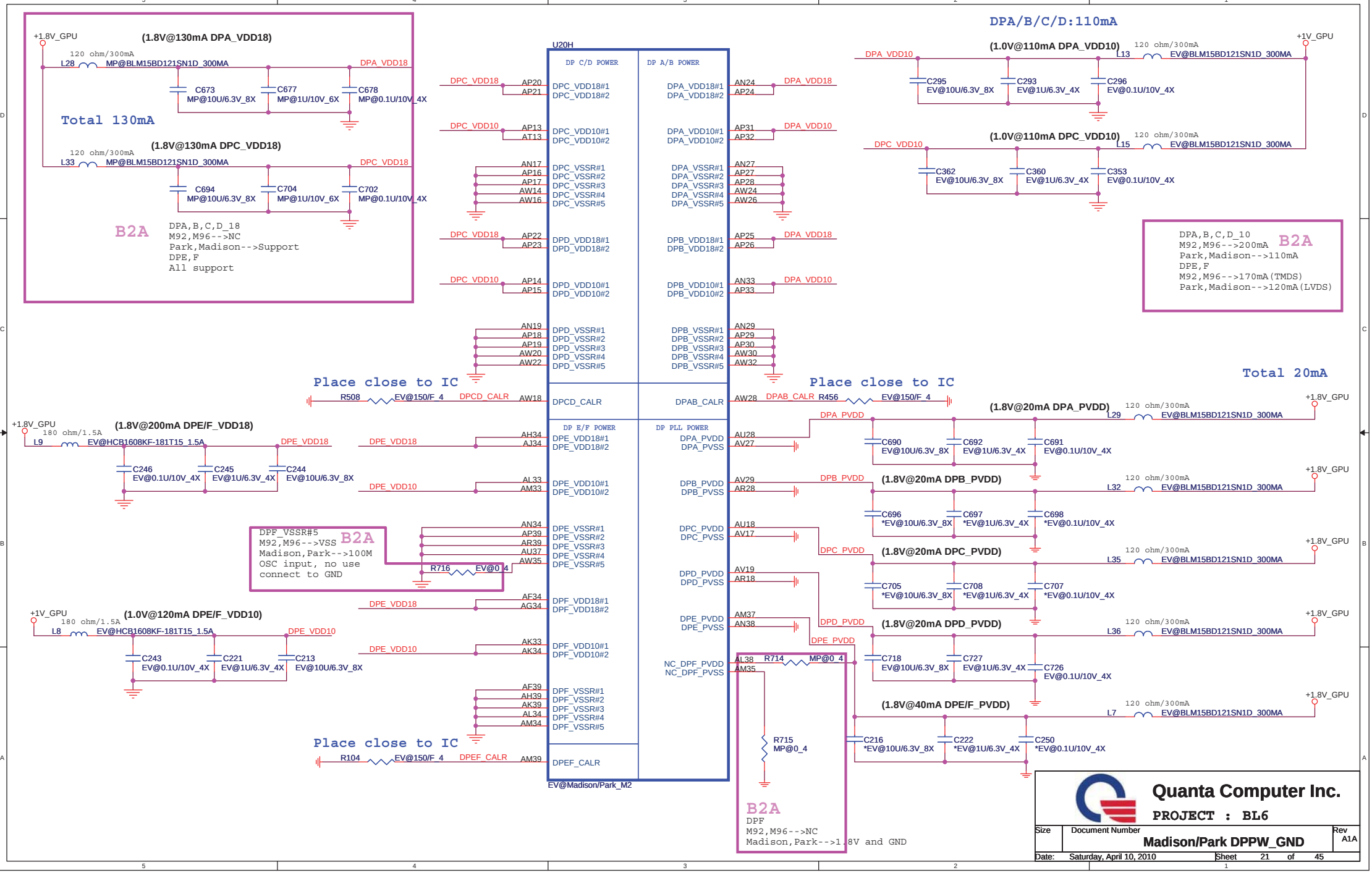
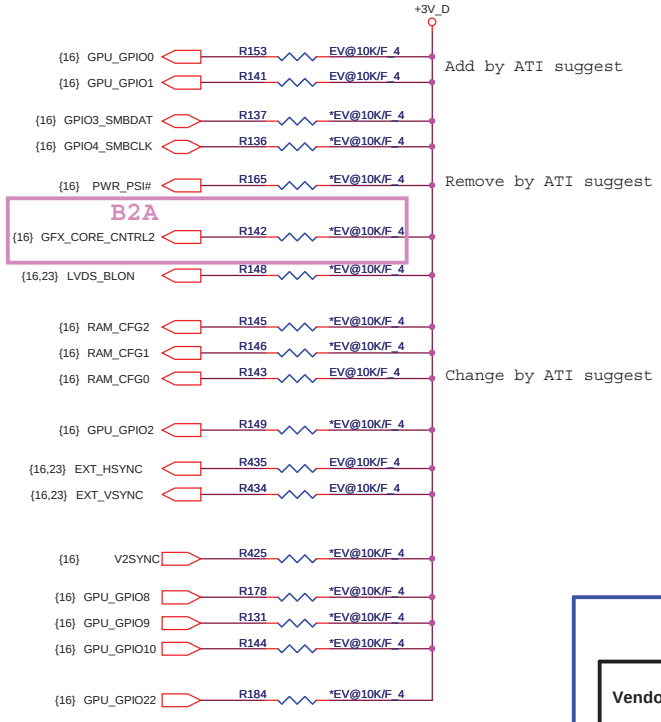


http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

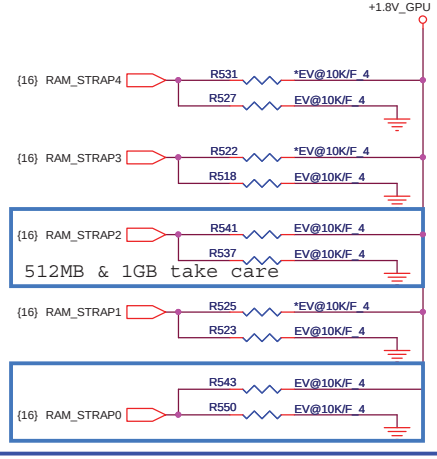
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

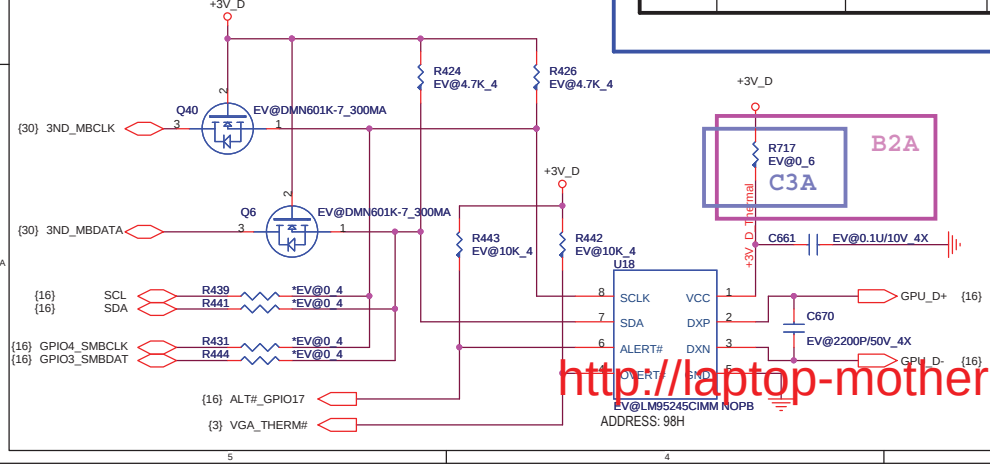
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

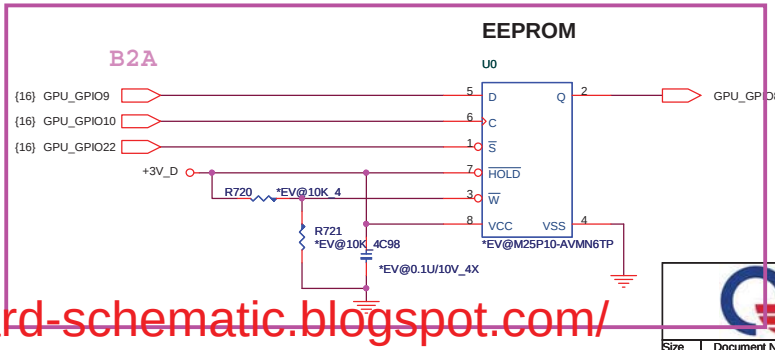
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B -HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



Thermal Sensor



EEPROM



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Size	Document Number	Rev
	Memory strip/Thermal/HDCP	A1A

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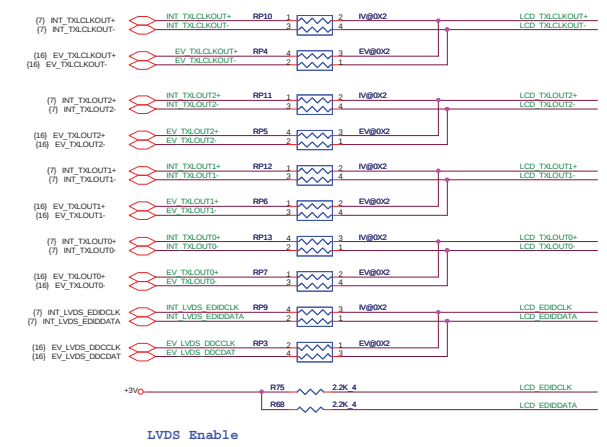
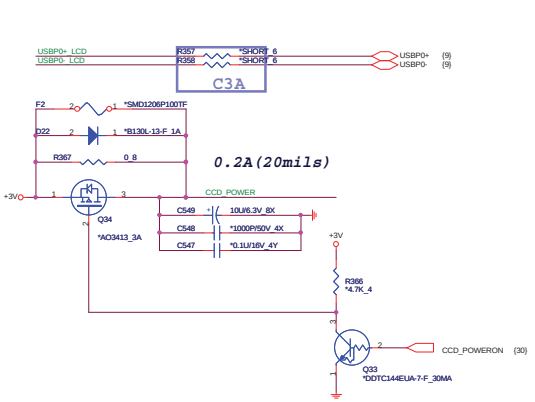
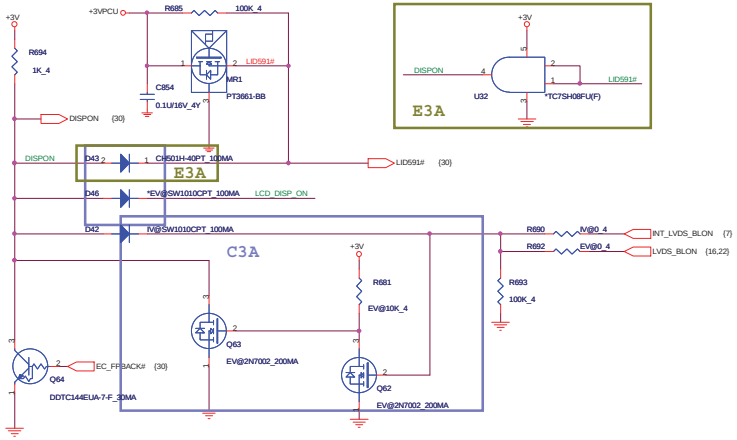
LVDS Signals



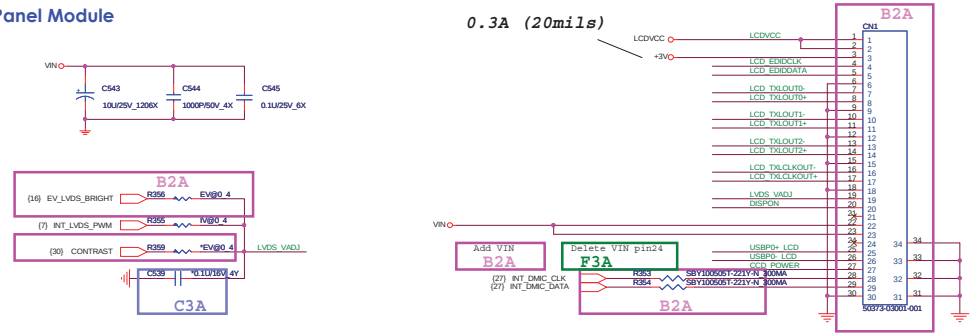
CCD



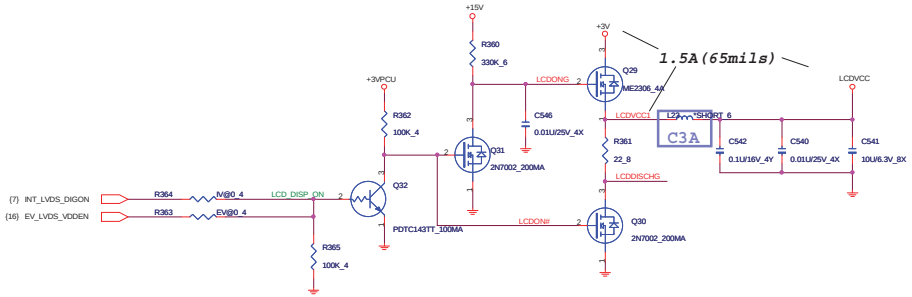
HALL SENSOR&BACK LIGHT SWITCH



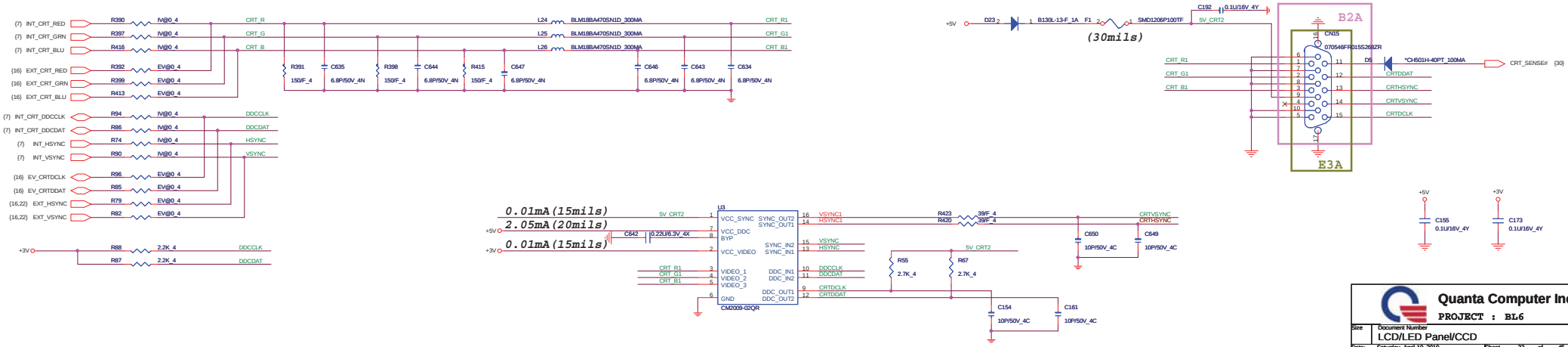
LCD Panel Module



LCD POWER SWITCH



CRT



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Size	Document Number	Rev
	LCD/LED Panel/CCD	A1A

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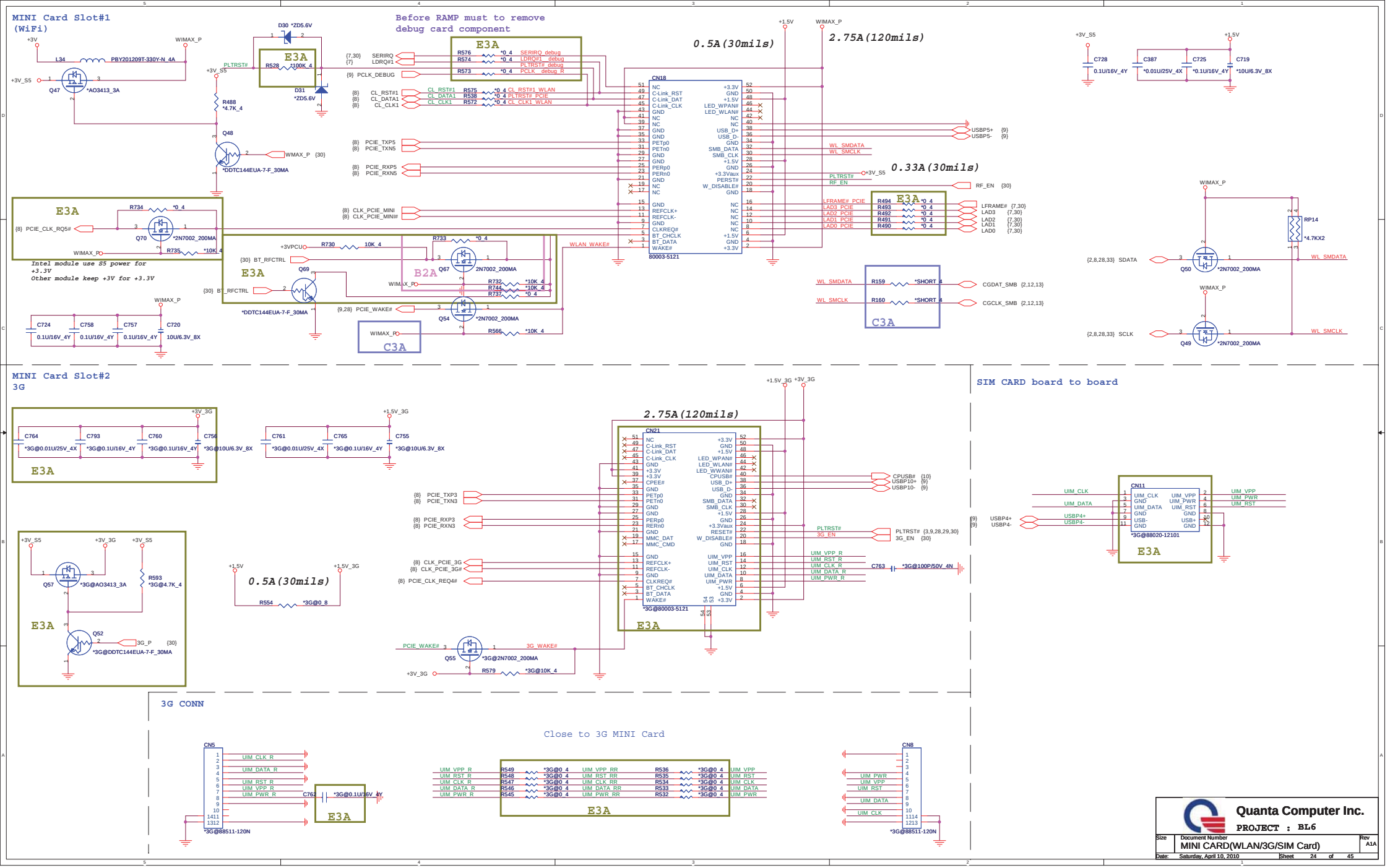
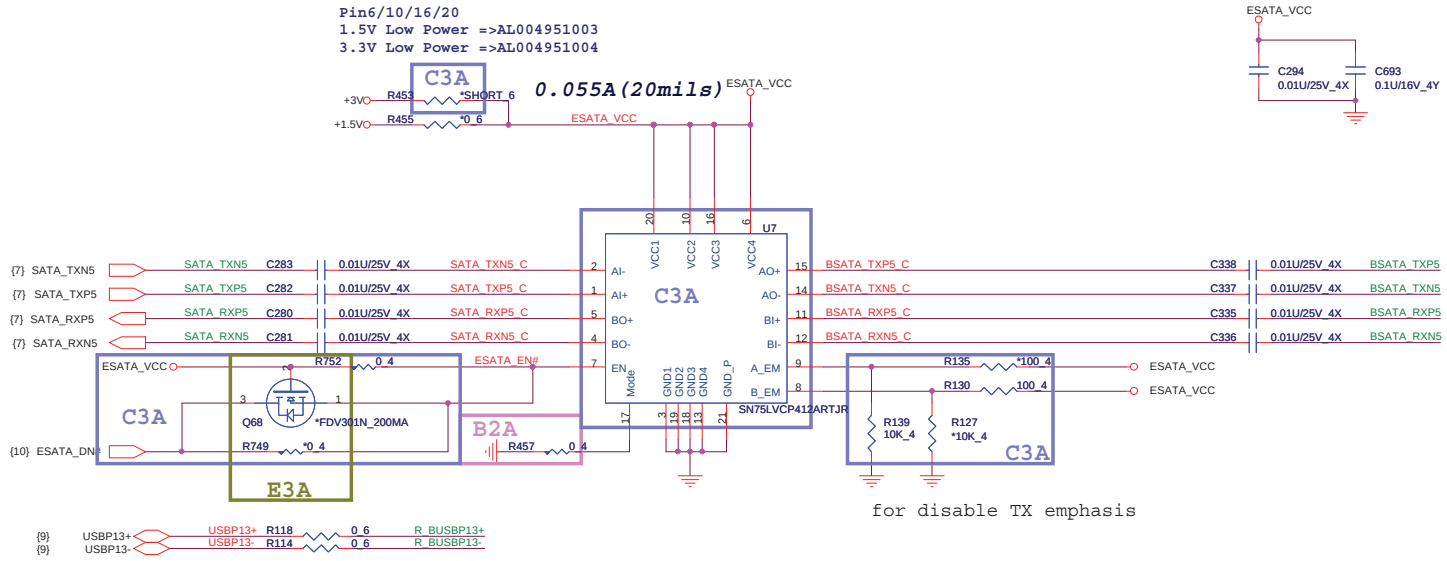


http://laptop-motherboard-schematic.blogspot.com/

ESATA Re-driver IC



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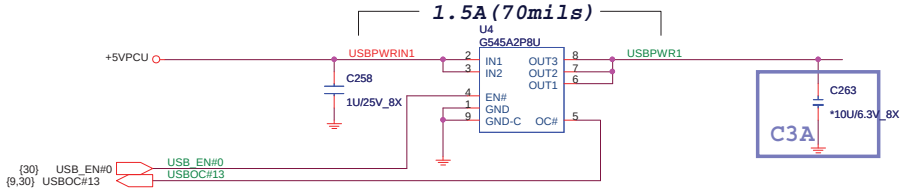
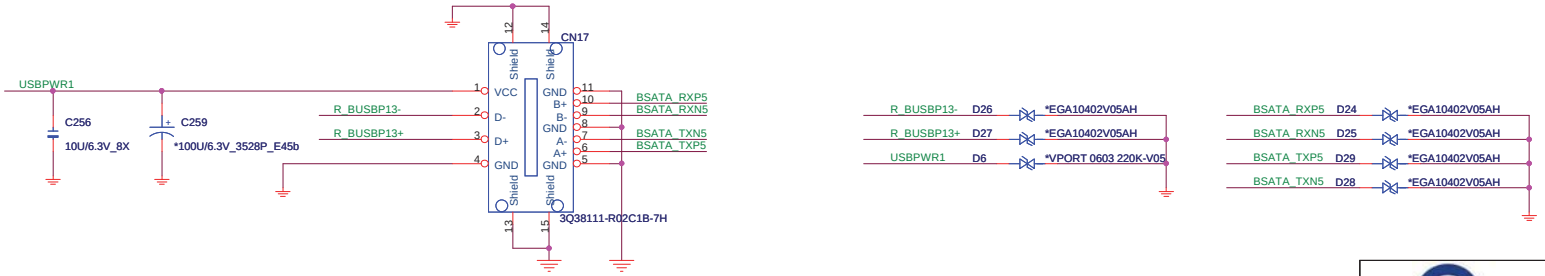


ESATA CONN



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Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	A1A

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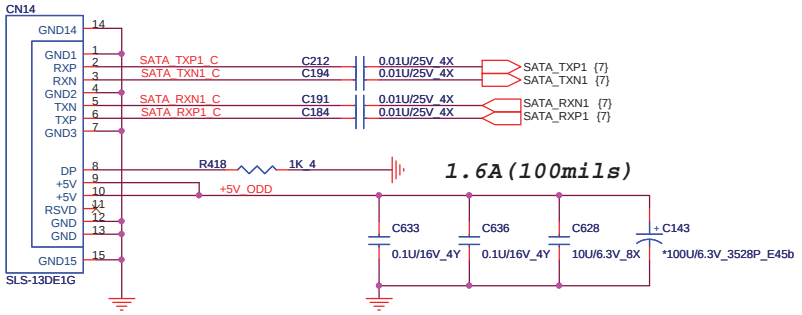
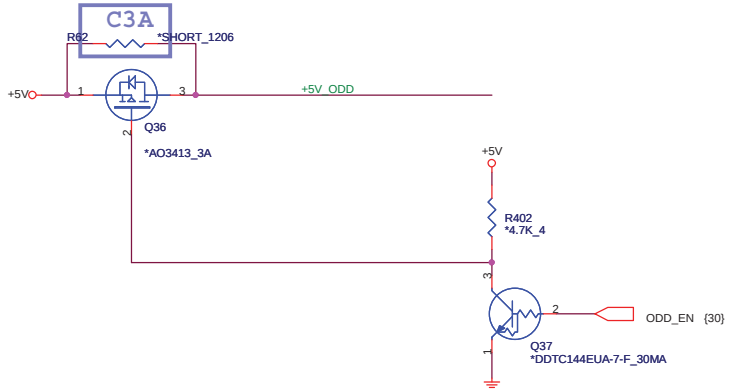
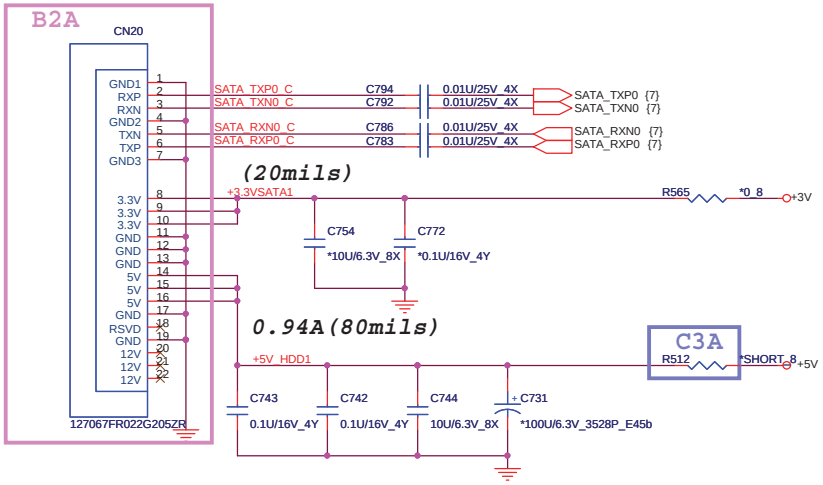
SATA ODD

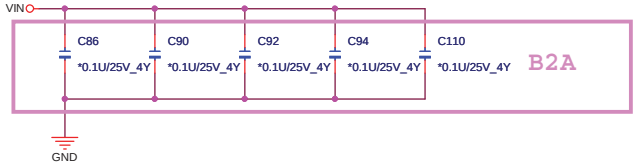


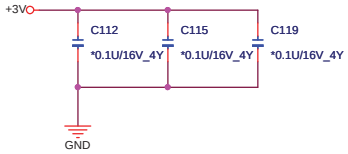


SATA HDD



EMI





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	HDD/ODD/EMI	A1A

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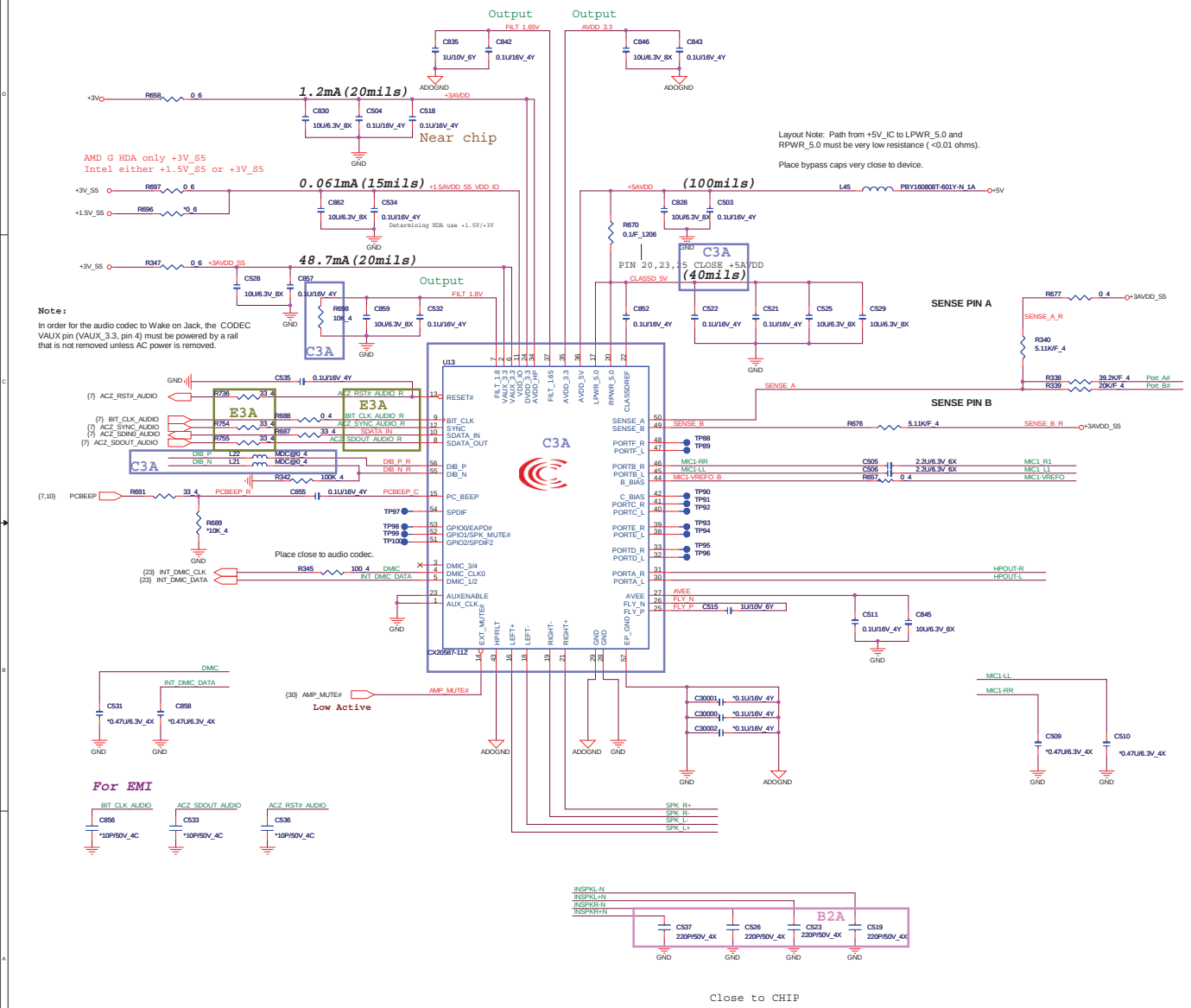
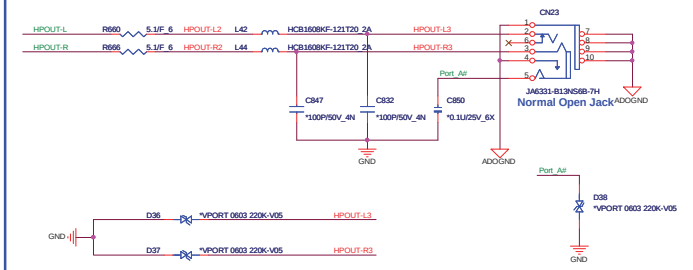
Codec (CX20587)

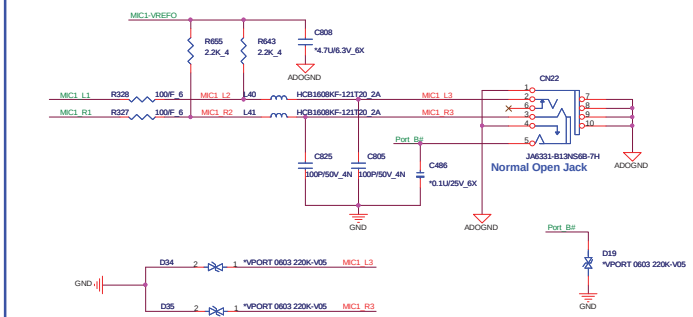


AUDIO JACKS

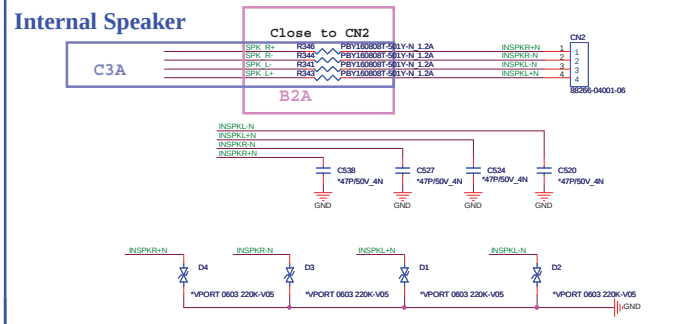
Earphone



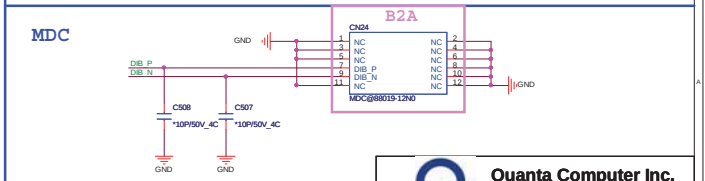
External MIC



Internal Speaker



MDC



Quanta Computer Inc.

PROJECT : BL6

Size | Document Number: Audio Codec (CX20583) | Rev: A1A

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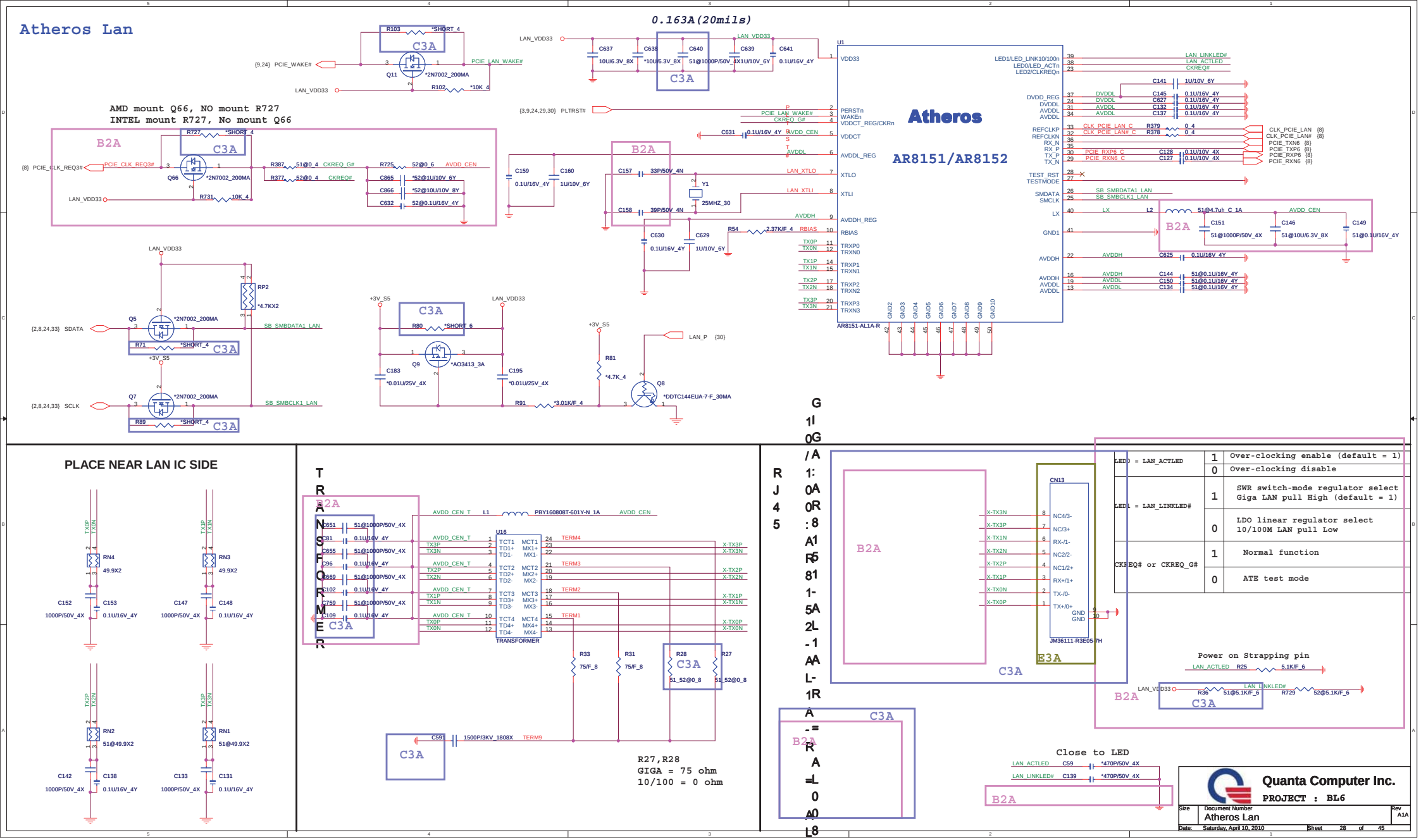
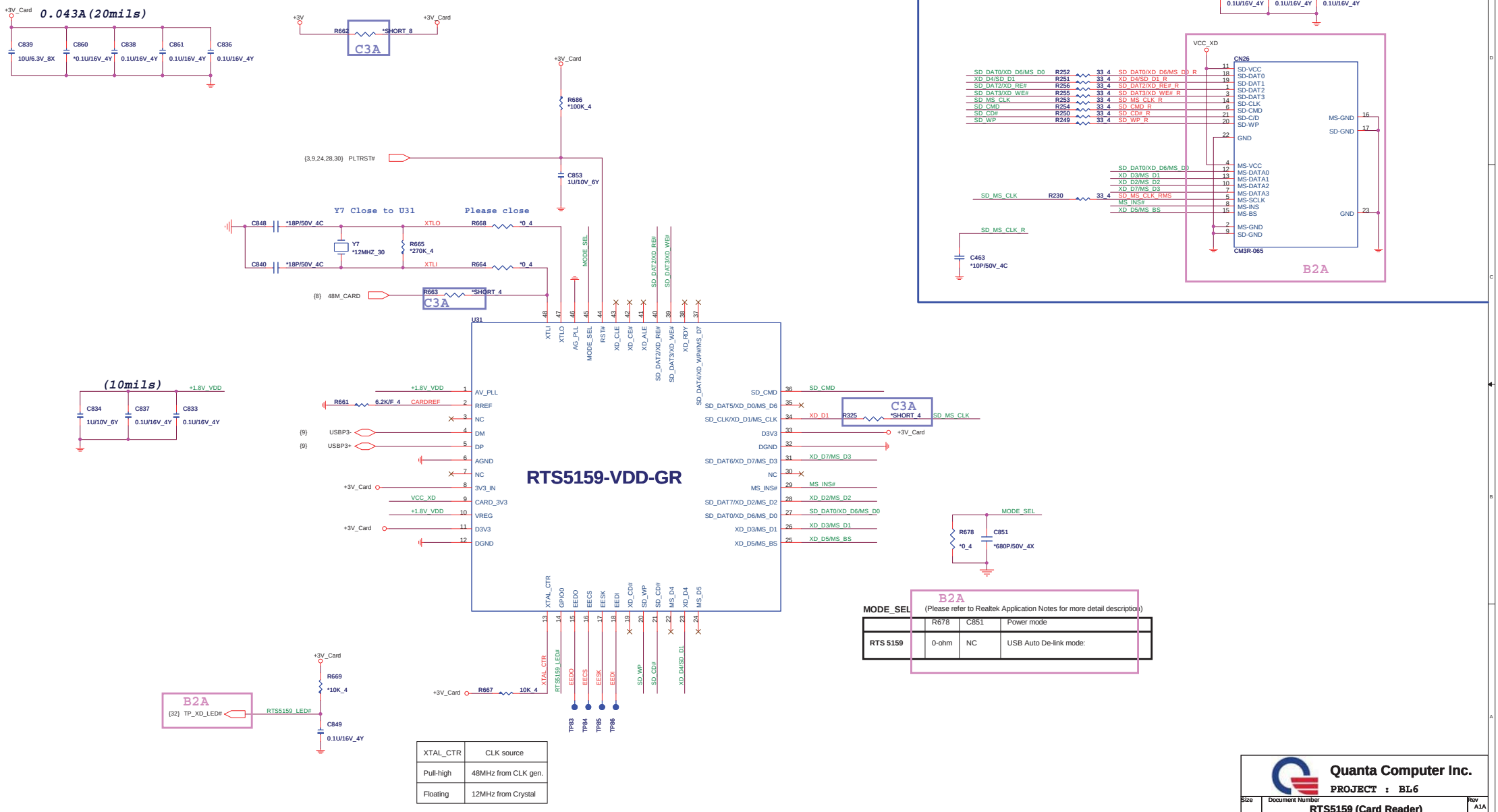
Atheros Lan



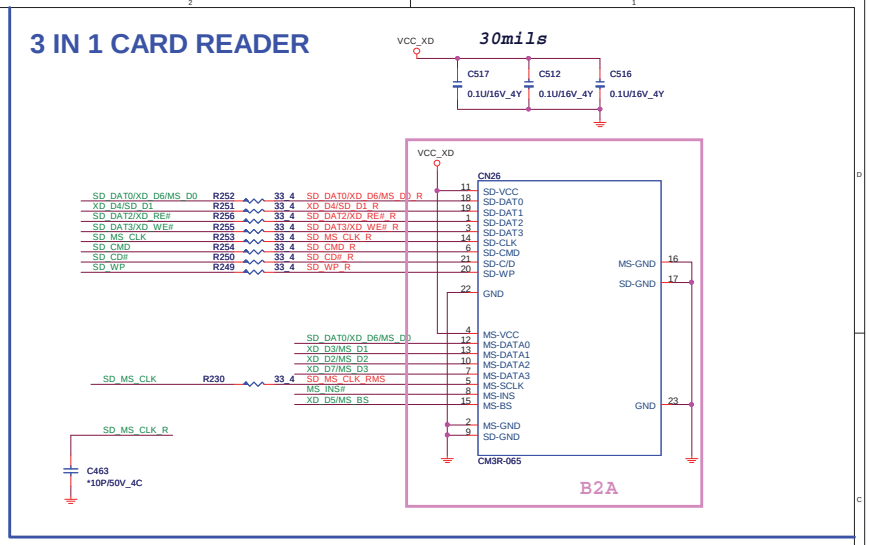
http://laptop-motherboard-schematic.blogspot.com/

5 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

3 IN 1 CARD READER



B2A

MODE_SEL (Please refer to Realtek Application Notes for more detail description)

	R678	C851	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	RTS5159 (Card Reader)	A1A

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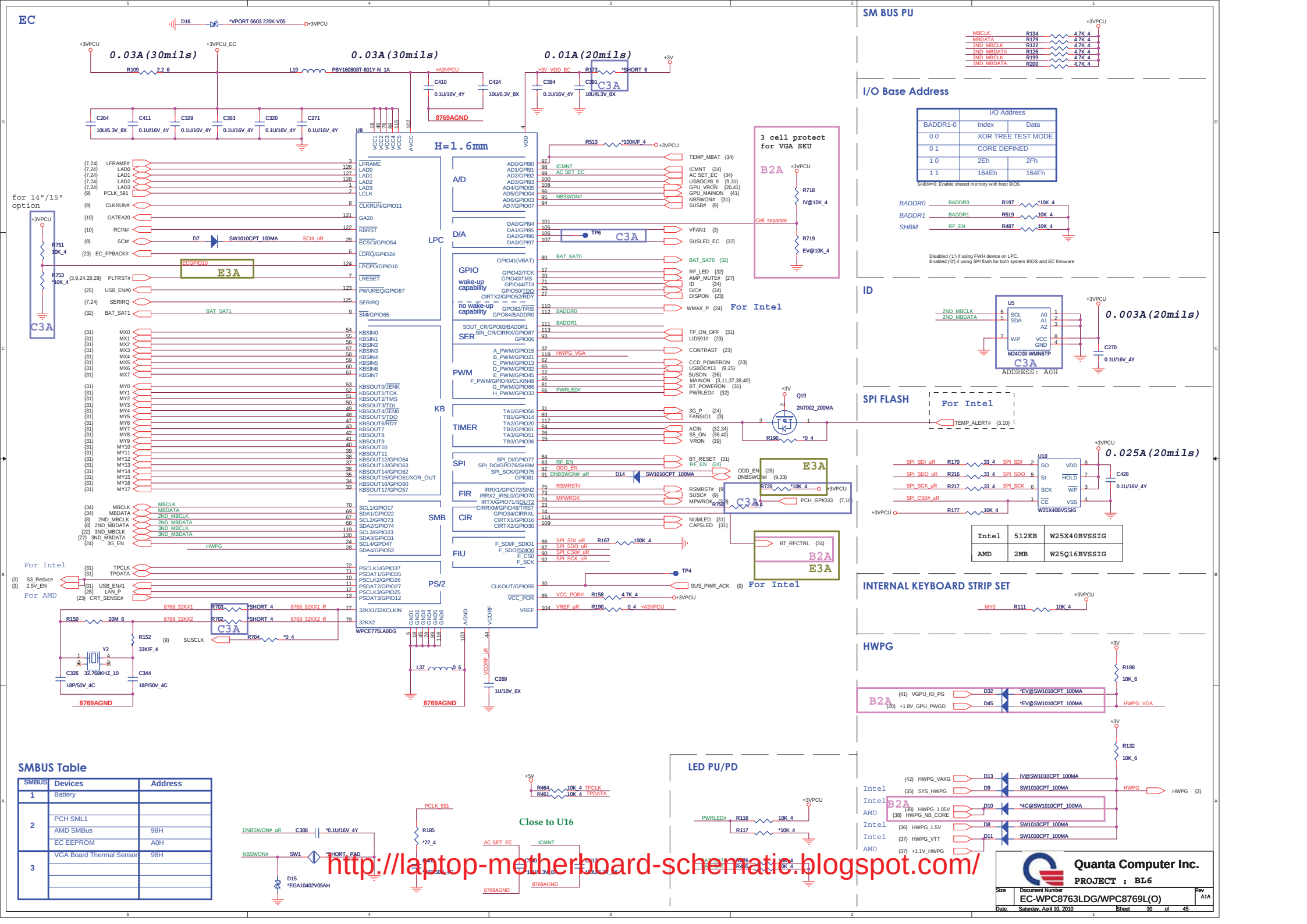

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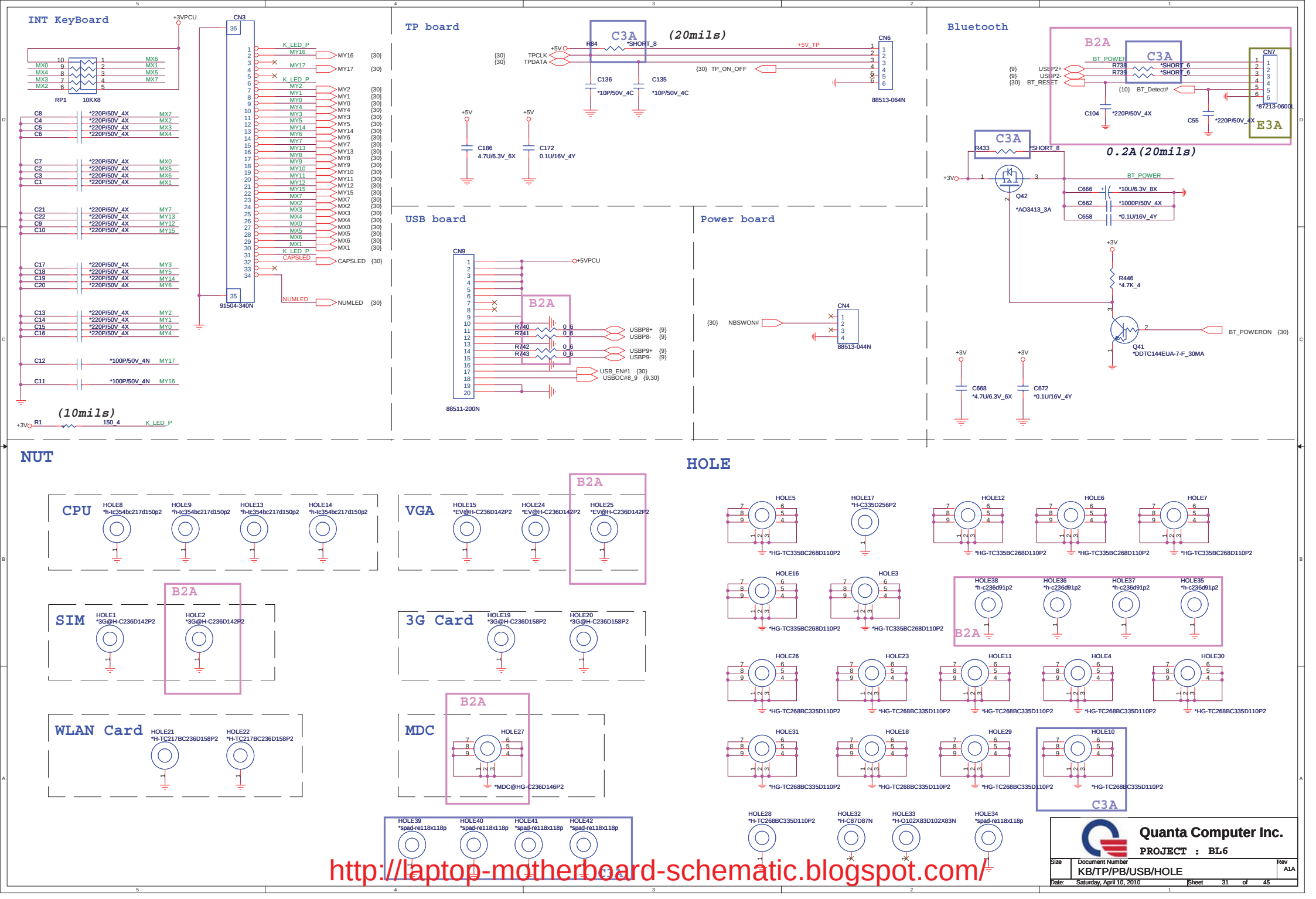
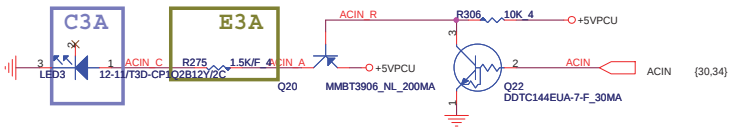


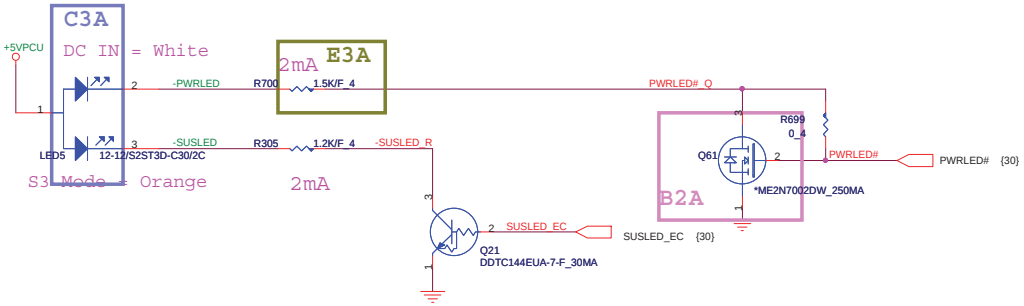
http://laptop-motherboard-schematic.blogspot.com/

LED

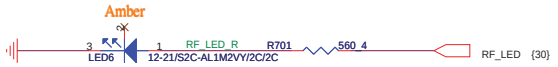
AC-IN



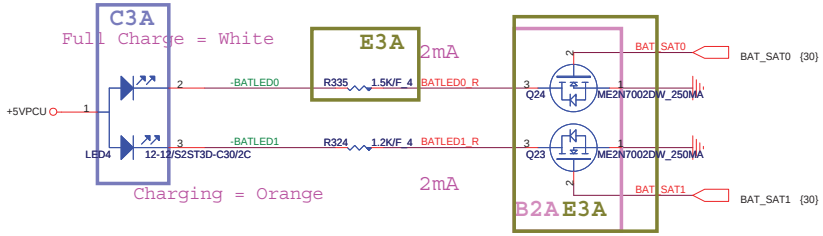
POWER



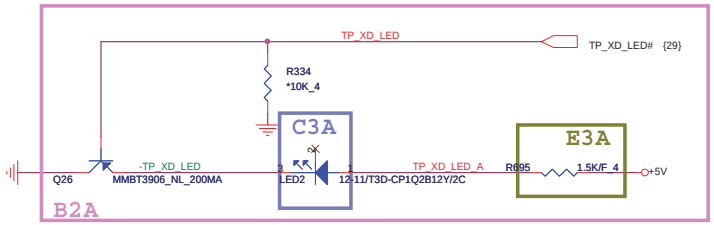
RF LED



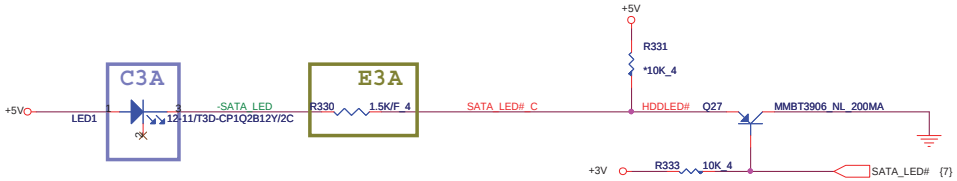
BATERRY



CARDREADER



HDD/ODD



ESD Protect

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Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	LED	A1A

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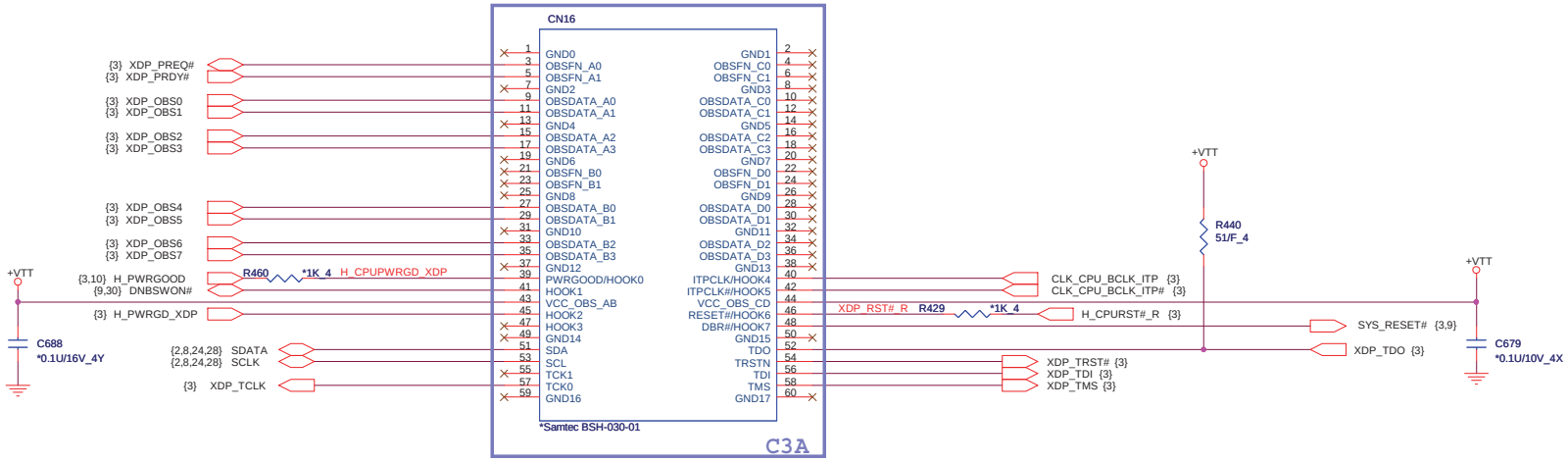
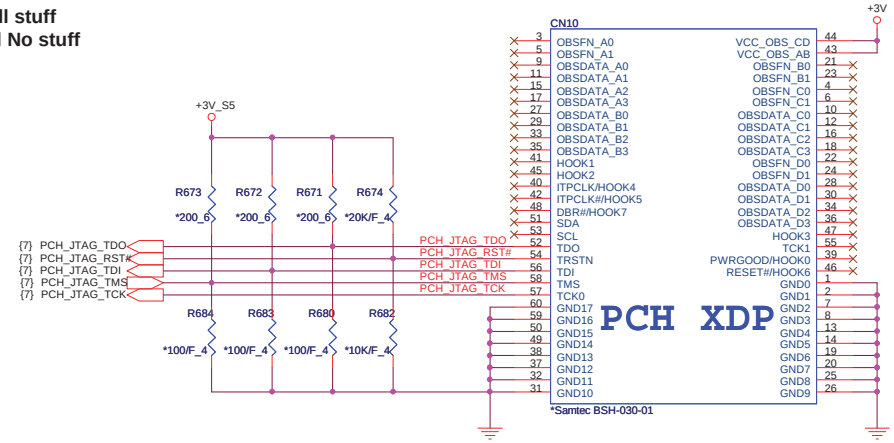
CPU XDP



Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

PCH XDP

Note: For ES1/ES2 version all stuff
Production version all No stuff



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Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	NVRAM Connector	A1A

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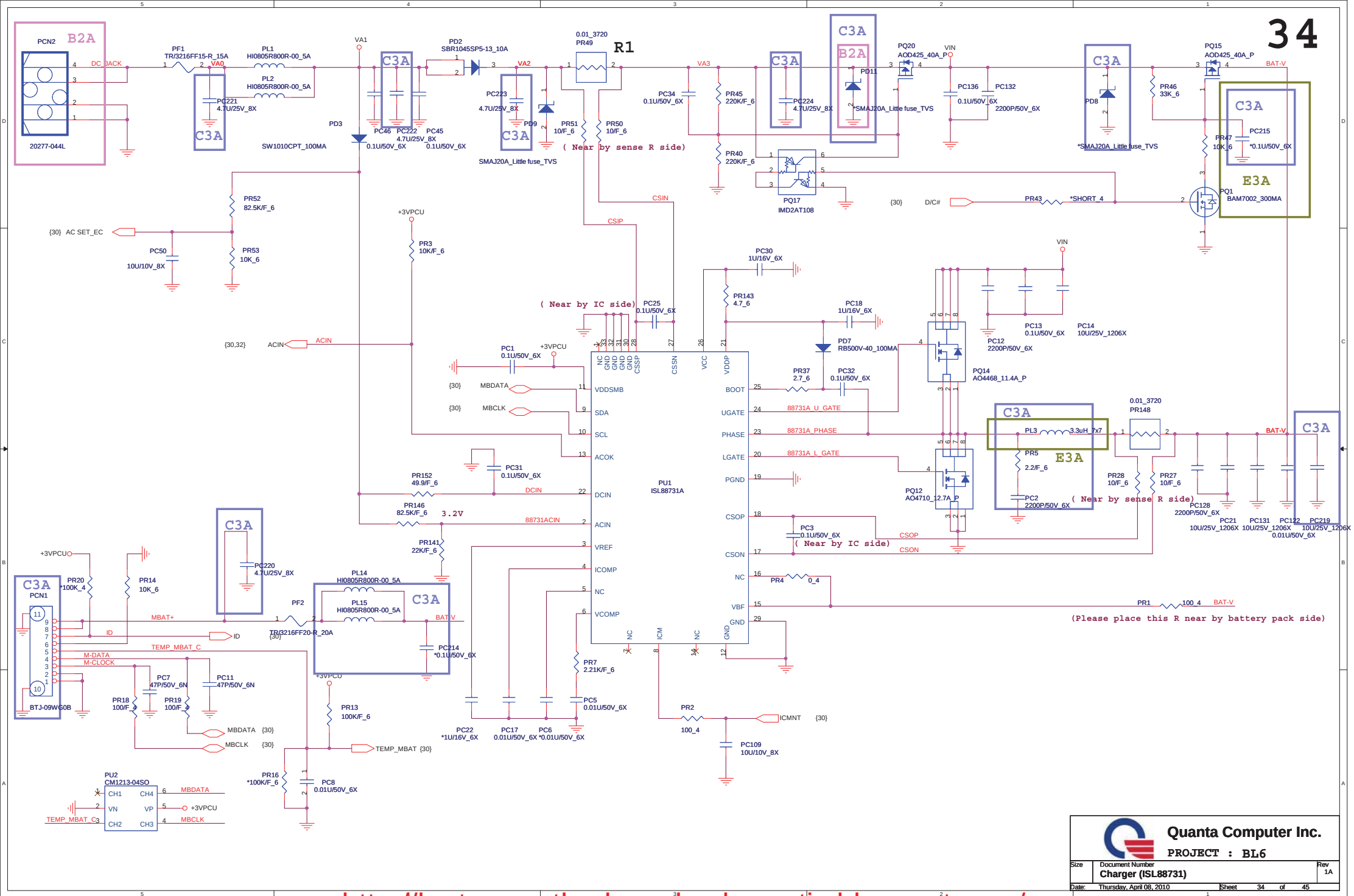

Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	Charger (ISL88731)	1A

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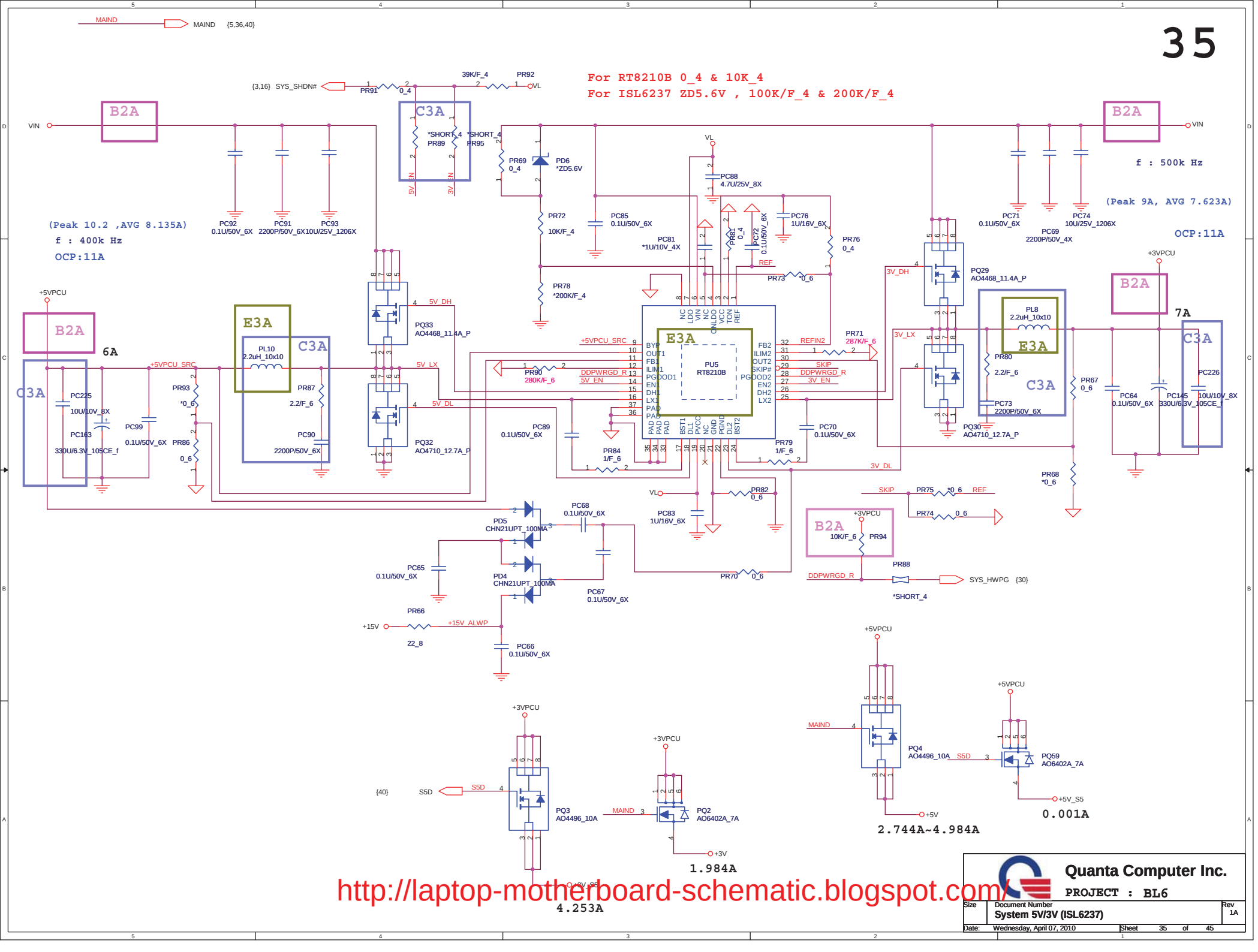
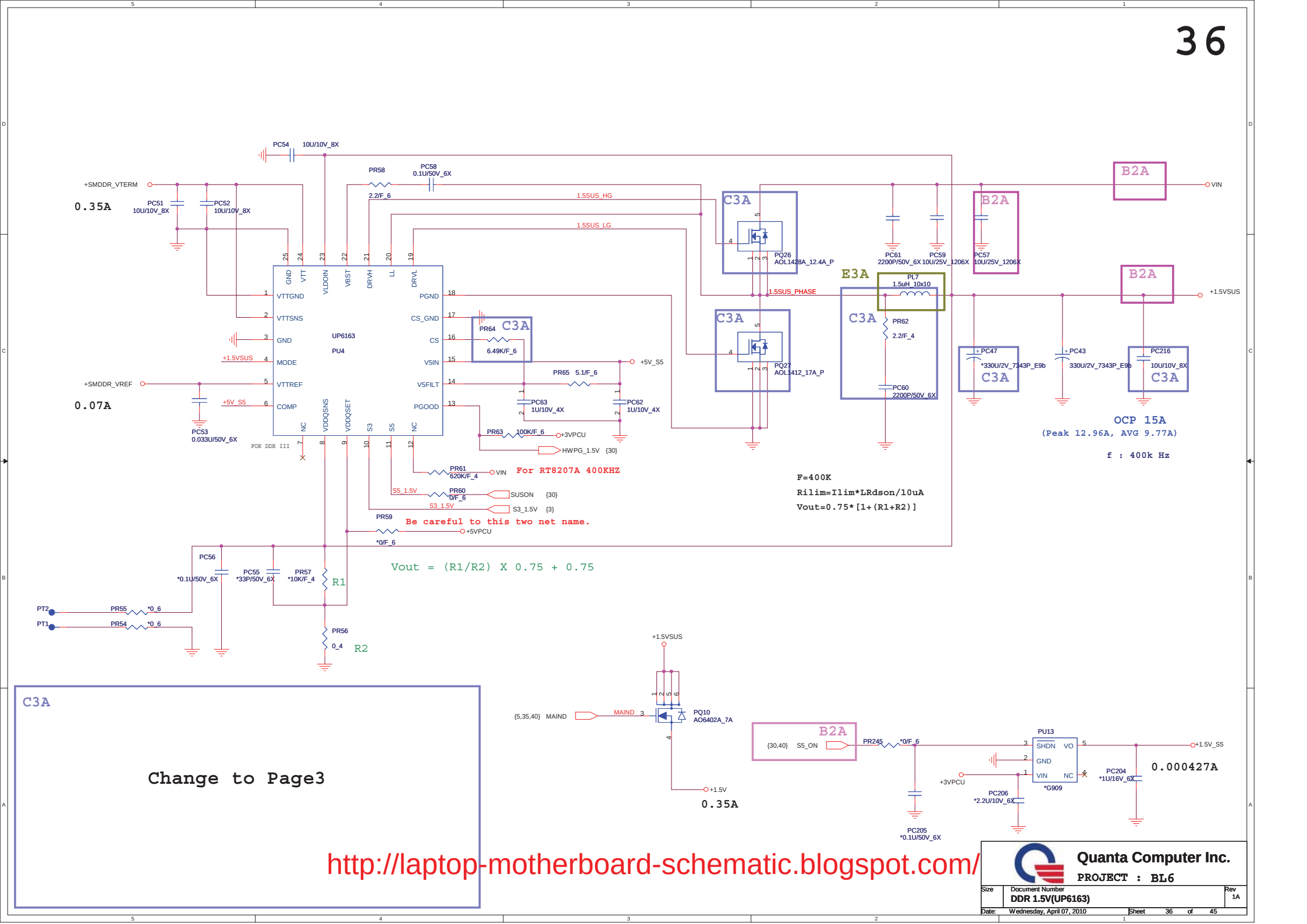
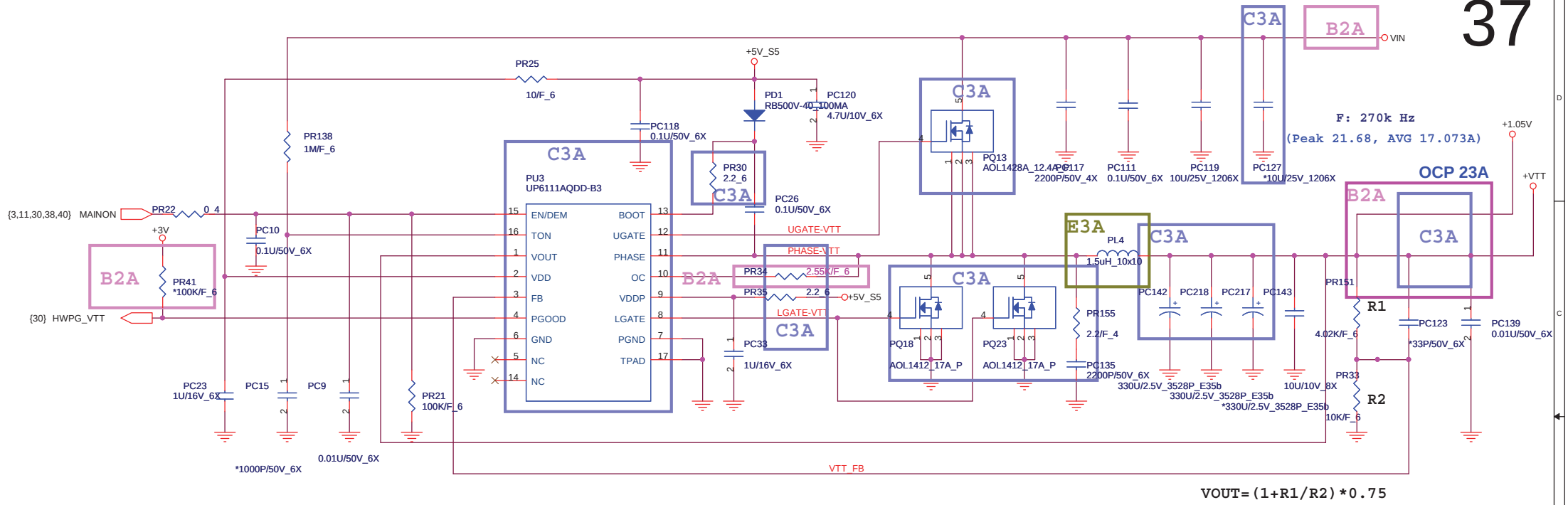


http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/



VOUT=(1+R1/R2)*0.75

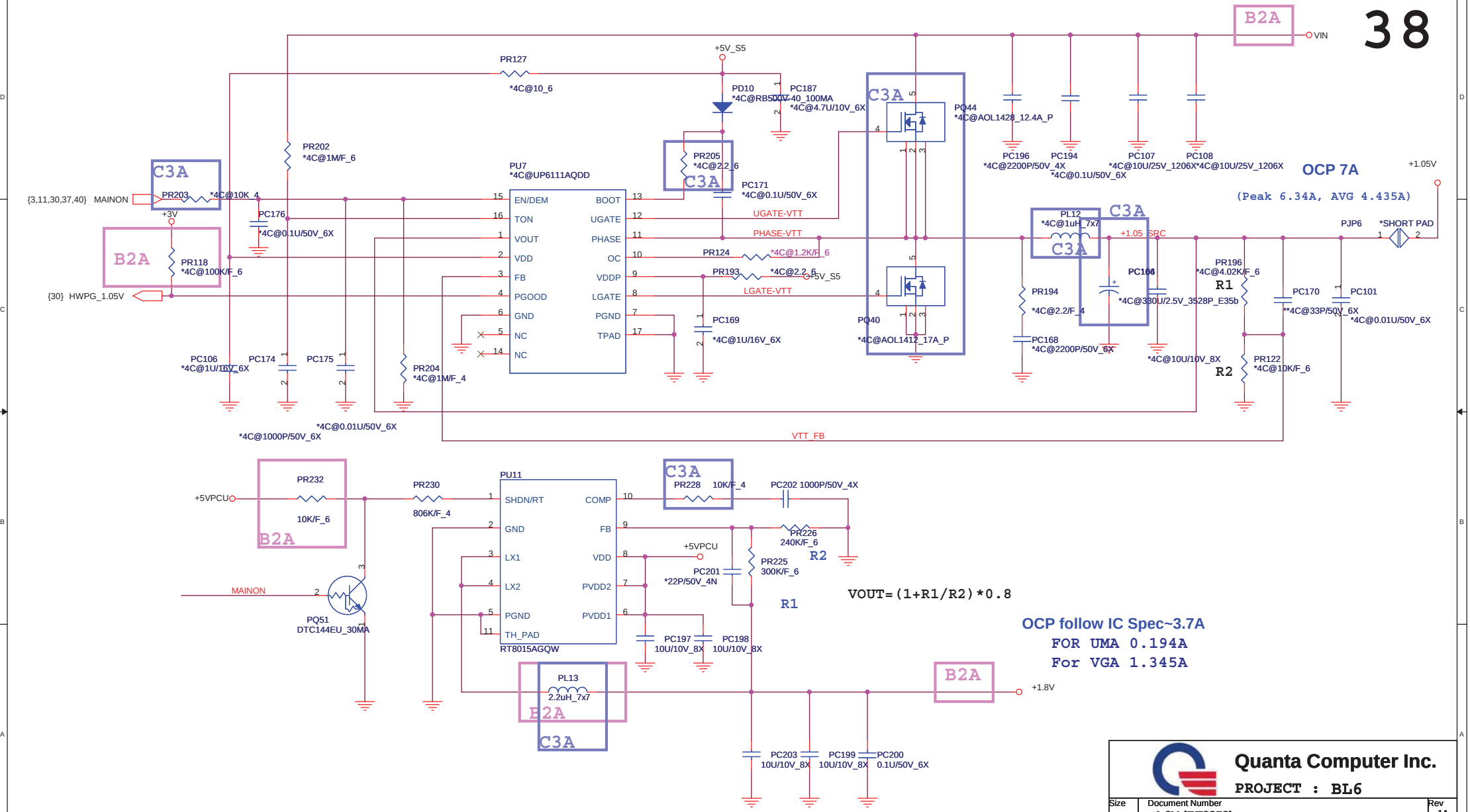
Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	+VTT (UP6111A)	1A

Date: Wednesday, April 07, 2010 Sheet 37 of 45

http://laptop-motherboard-schematic.blogspot.com/



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PROJECT : BL6

Size	Document Number	Rev
	+1.8V (RT8253)	1A

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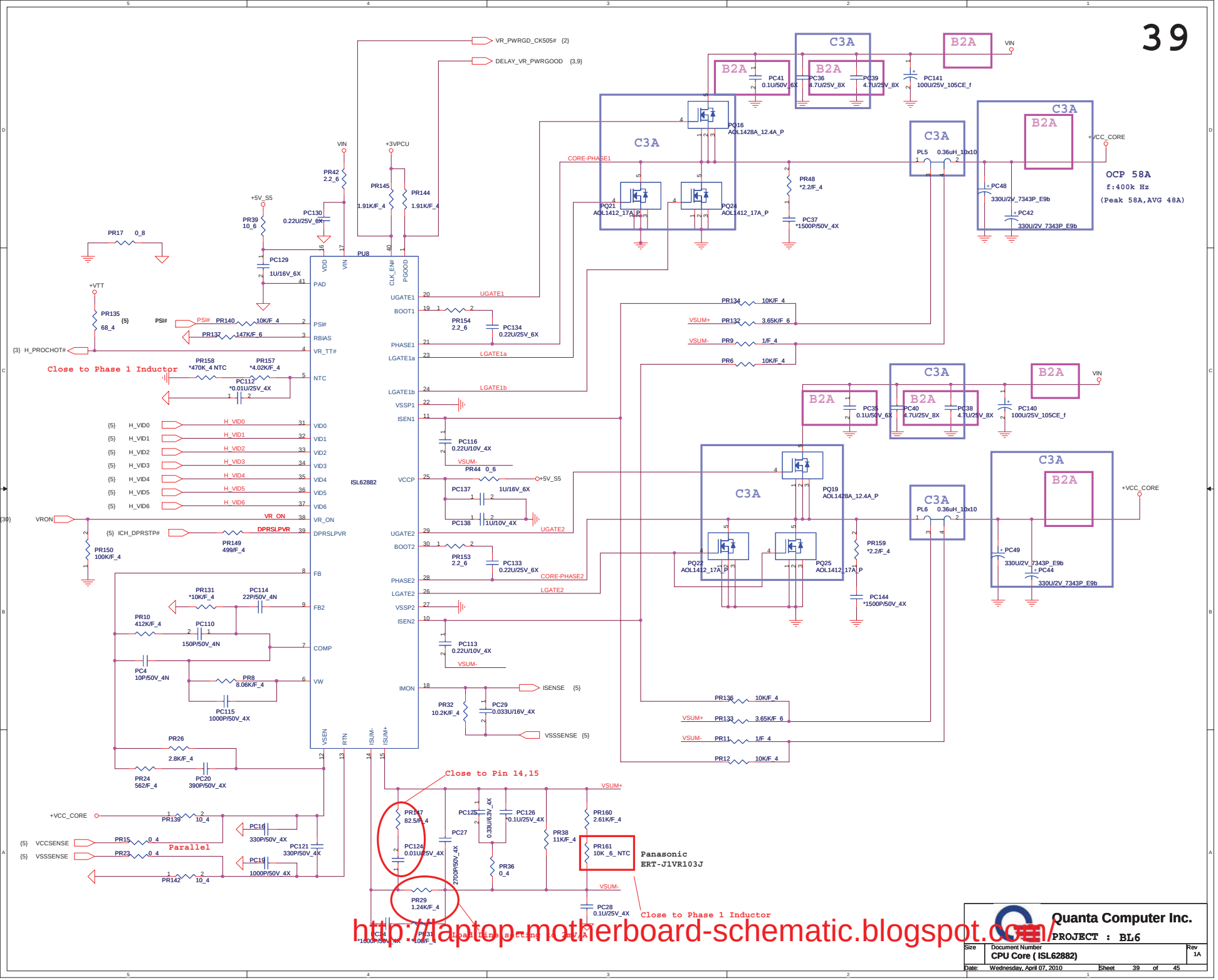
http://laptop-motherboard-schematic.blogspot.com/



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Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	CPU Core (ISL62882)	1A

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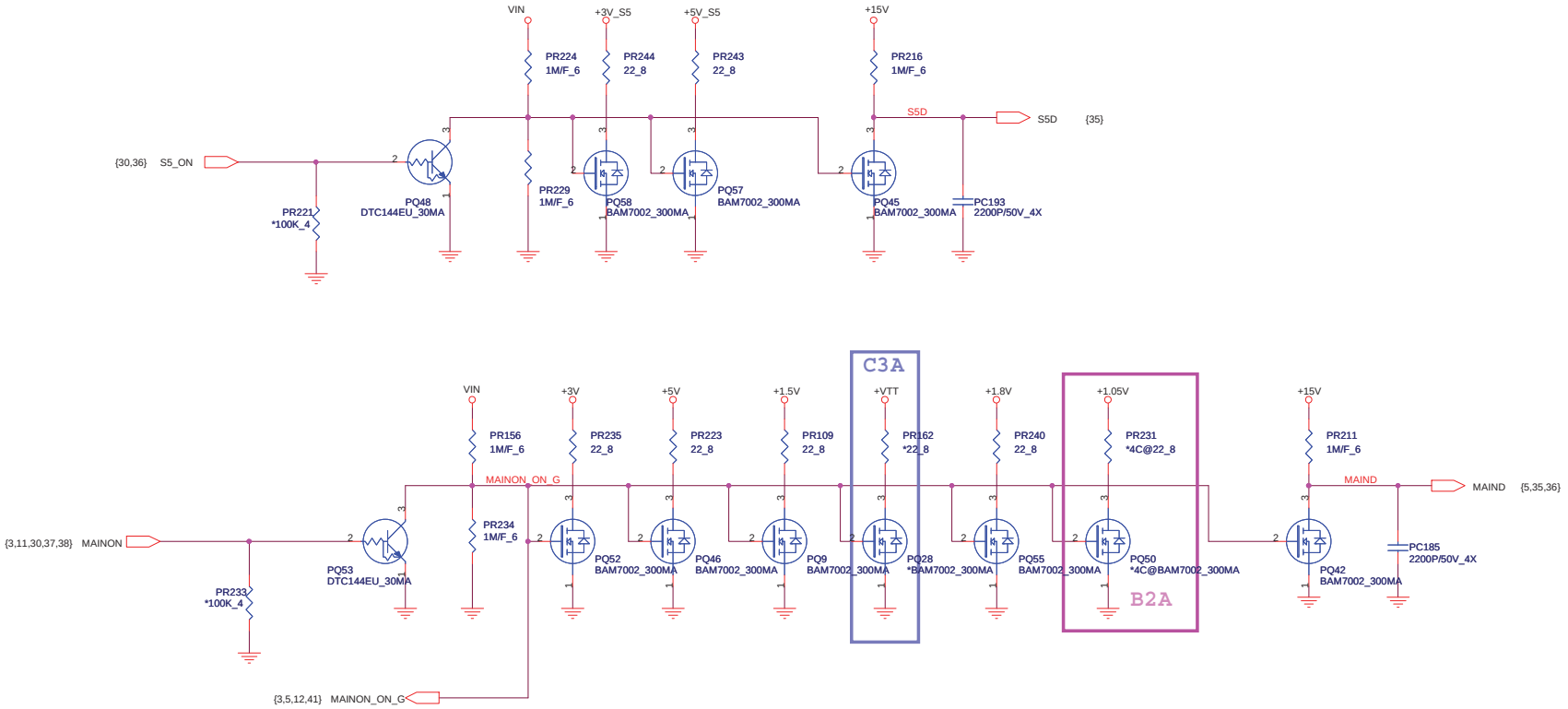


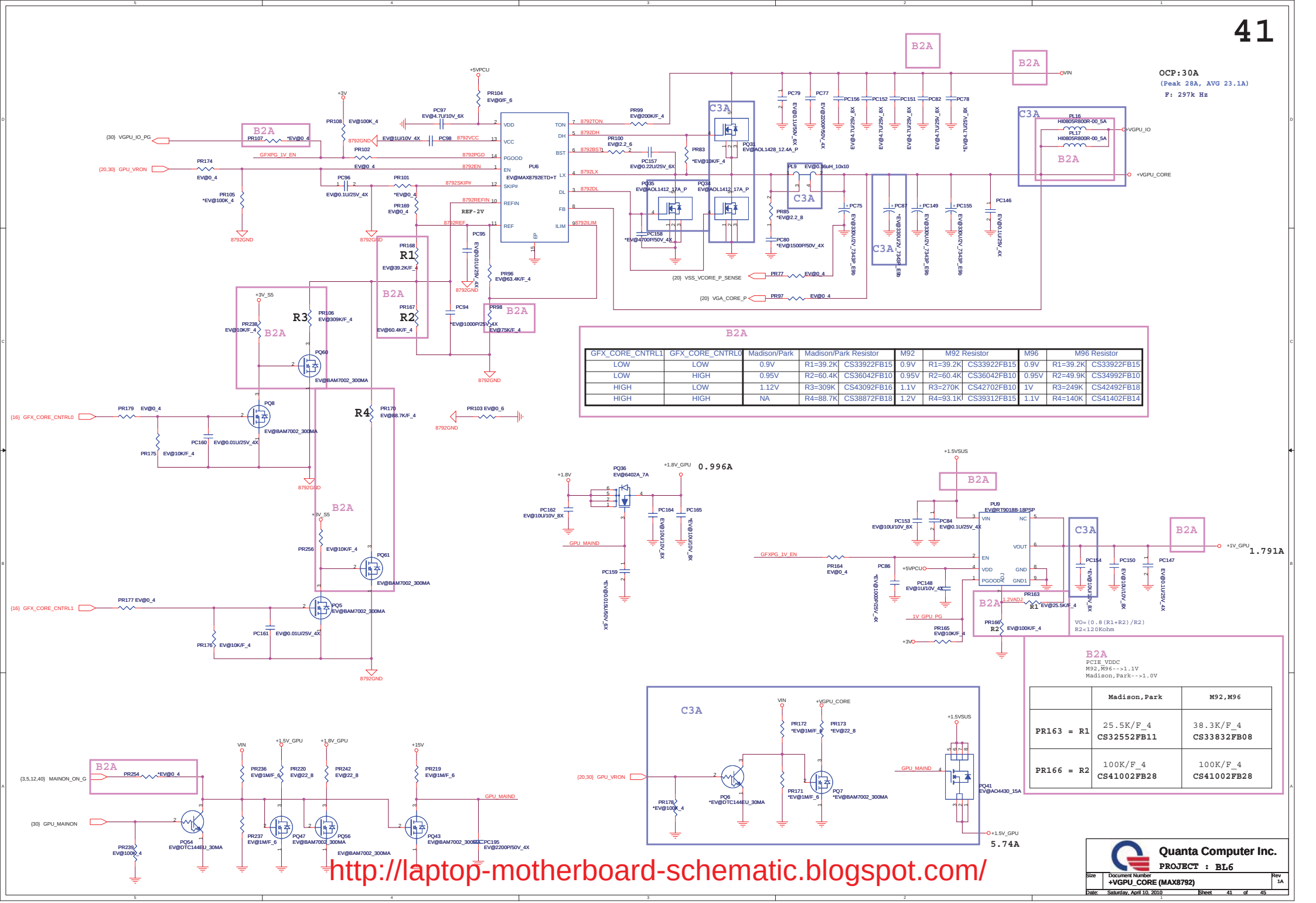
http://laptop-motherboard-schematic.blogspot.com/

Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	1A

Date: Wednesday, April 07, 2010 Sheet 40 of 45



B2A

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	Madison/Park	Madison/Park Resistor		M92	M92 Resistor		M96	M96 Resistor	
LOW	LOW	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15
LOW	HIGH	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=49.9K	CS34992FB10
HIGH	LOW	1.12V	R3=309K	CS43092FB16	1.1V	R3=270K	CS42702FB10	1V	R3=249K	CS42492FB18
HIGH	HIGH	NA	R4=88.7K	CS38872FB18	1.2V	R4=93.1K	CS39312FB15	1.1V	R4=140K	CS41402FB14

B2A
PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR163 = R1	25.5K/F_4 CS32552FB11	38.3K/F_4 CS33832FB08
PR166 = R2	100K/F_4 CS41002FB28	100K/F_4 CS41002FB28

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Quanta Computer Inc.
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Size	Document Number	Rev
	+VGPU_CORE (MAX8792)	1A

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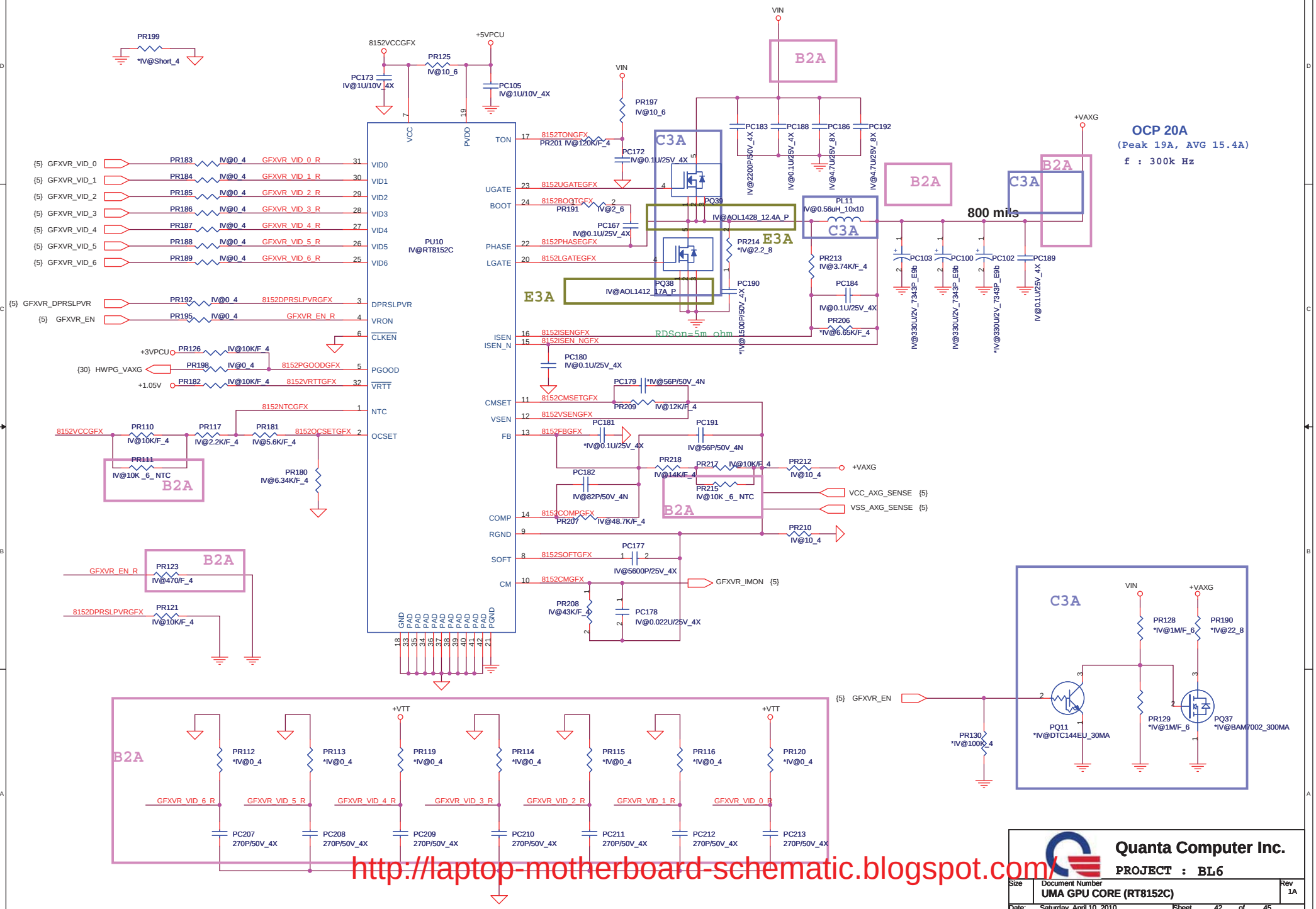

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Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	UMA GPU CORE (RT8152C)	1A

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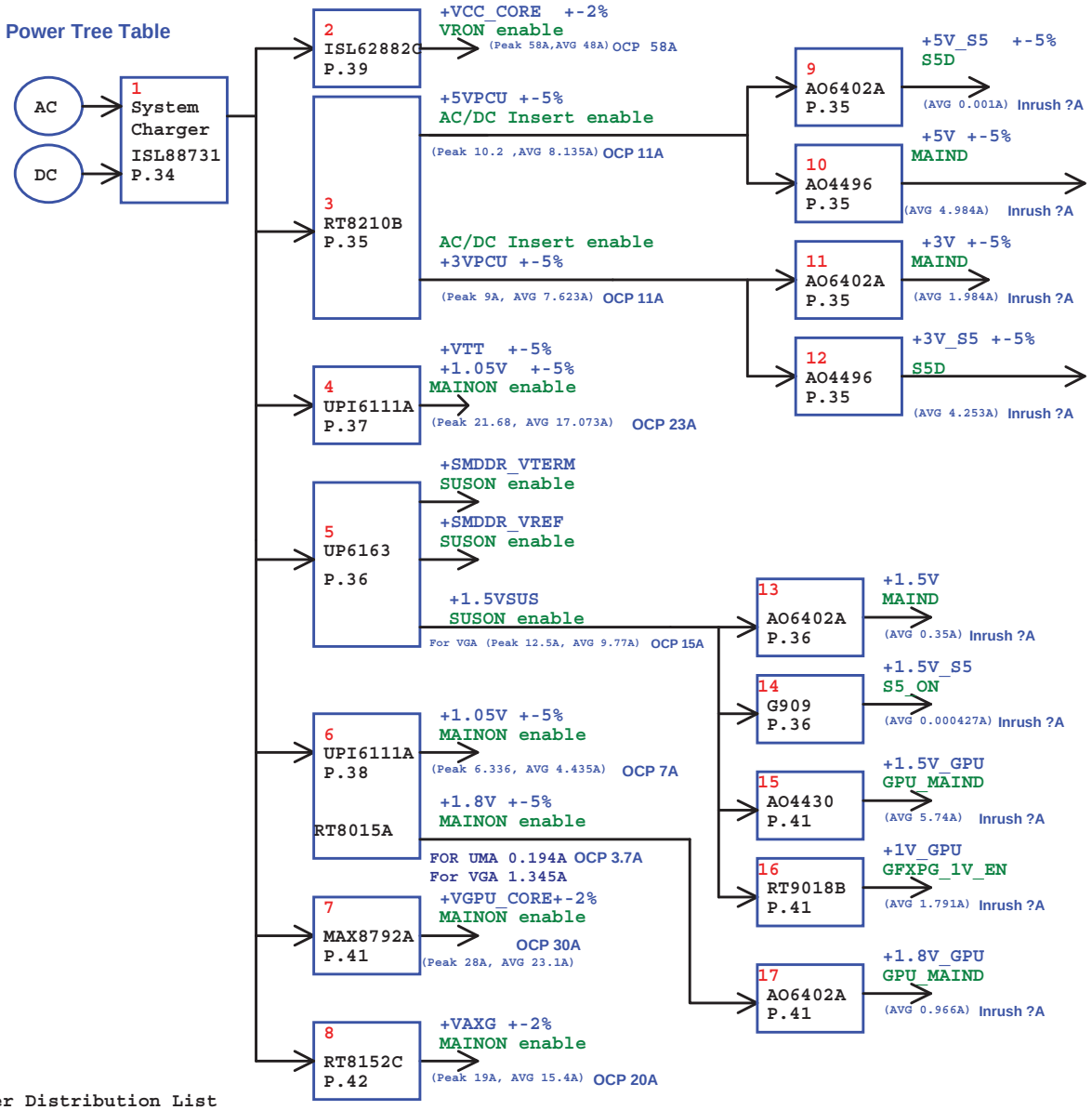
Power Tree Table



Power Distribution List

Power	Distribution

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